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Presentations and demos

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Preface

Dear participant,

It is a pleasure to welcome you to the ESI Symposium 2008.

In your hands are the participant's proceedings of the first ESI Symposium that is not devoted to a particular ESI project. Instead, it has been organized to report on all main developments at ESI in an integral manner. The reason for this is at least twofold: first, ESI has now grown to the size where the organisation of specific symposia for each project would create too great a load for both audience and organisers; second, the true value of the ESI research agenda is best appreciated by the common themes, approaches and results across the different projects, and are most naturally communicated as part of a general symposium.

So, in some way this symposium marks the coming of age of ESI as a research institute, and it is customary to invite friends and relatives at such memorable occasions. In the programme you will therefore find not only reports on the activities of ESI, but also presentations by our colleagues of NIRICT/CeDICT of 3TU, the Dutch federation of technical universities, and presentations related to PROGRESS, the embedded systems research programme of the Netherlands Organisation for Scientific Research NWO, the Dutch Technology Foundation STW, and the Ministry of Economic Affairs.

Of course, our symposium would not be complete without renowned keynote speakers. I am delighted that Lothar Thiele of the ETH Zürich and Anton Schaaf of Océ have agreed to shed their light on important developments form the perspectives of a leading academic researcher, and a leading industrialist, respectively. Finally, ESI itself will also rise to the occasion and present its plans and visions for the future.

In addition to the presentations, there will be an exciting market with demonstrators and posters that will give an excellent impression of the results that have been achieved so far. All together, I hope that you will find it a stimulating and rewarding programme of the many activities in and around ESI, providing a basis for future collaboration.

I would like to thank everybody who has contributed to make this symposium a reality, especially the keynote speakers, the speakers, the demonstrators and the support staff. And I thank you, dear participant, for attending this symposium and wish you a pleasant, informative and fruitful day.

Sincerely,

Ed Brinksma
Scientific Director and Chair
Embedded Systems Institute

Contents

Abstracts

Keynote presentation 1:

Predictability and efficiency in wireless sensor networks

Abstract: Recently, there has been lots of interest in various aspects of wireless sensor networks. They can be characterized by a potentially large number of individual nodes that perform sensor, computation and communication tasks. These small embedded systems are interconnected via wireless links.

Application domains can be found in environmental monitoring, logistics, security, safety, health and building automation.

Much of the research and development effort in this area has been devoted to increase the efficiency of these massively distributed embedded systems in terms of computing power, memory space, communication bandwidth and energy. On the other hand, predictability of the system functionality in terms of functionality, timing and battery lifetime has only been of secondary interest.

The talk covers several novel techniques that can be used to design predictable and efficient large scale distributed embedded systems. Two application scenarios will be described where these methods have been successfully applied.

About the speaker: Lothar Thiele was born in Aachen, Germany on April 7, 1957. He received his Diplom-Ingenieur and Dr.-Ing. degrees in Electrical Engineering from the Technical University of Munich in 1981 and 1985 respectively. After completing his Habilitation thesis from the Institute of Network Theory and Circuit Design of the Technical University Munich, he joined the Information Systems Laboratory at Stanford University in 1987.

In 1988, he took up the chair of microelectronics at the Faculty of Engineering, University of Saarland, Saarbrucken, Germany. He joined ETH Zurich, Switzerland, as a full Professor of Computer Engineering, in 1994. He is leading the Computer Engineering and Networks Laboratory of ETH Zurich.

His research interests include models, methods and software tools for the design of embedded systems, embedded software and bio-inspired optimization techniques.

In 1986 he received the Dissertation Award of the Technical University of Munich, in 1987, the Outstanding Young Author Award of the IEEE Circuits and Systems Society, in 1988, the Browder J. Thompson Memorial Award of the IEEE, and in 2000-2001, the IBM Faculty Partnership Award. In 2004, he joined the German Academy of Natural Scientists Leopoldina. In 2005, he was the recipient of the Honorary Blaise Pascal Chair of University Leiden, The Netherlands.

Keynote presentation 2:

Innovation acceleration, the way with ESI

About the speaker: Anton Schaaf (1954, The Netherlands) worked from 1987 till 2005 at Siemens AG and had a variety of functions all over the world. He acted as an executive vice president, member of the board of directors and as the Chief Technology Officer for Siemens Communications in Germany. From 2005 on, he held the position of Chief Technology Officer at Deutsche Telekom AG.

Since July 1st, 2006, he joined Océ N.V. in The Netherlands as the Chief Technology and Operations Officer and since October 11th, 2006, he was appointed member of the board of directors.

1.1 User-perceived reliability of high-volume products

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Abstract: The reliability of high-volume products, such as consumer electronic devices, is threatened by the combination of increasing complexity, decreasing time-to-market, and strong cost constraints. To maintain a high level of reliability and to avoid customer complaints, the Trader project proposes a number of methods and techniques. Part of the Trader results aim at the detection of faults and product weaknesses during development. This includes requirements modelling, source code analysis, and stress testing. To improve reliability after release, a runtime awareness concept has been proposed, similar to the classical feedback control loop. It gives the system a kind of awareness that its customer-perceived behaviour is – or is likely to become – erroneous. In addition, the system should have a strategy to correct itself in line with customer expectations.

The main ingredients of such a run-time awareness and correction approach are depicted in Figure 1.

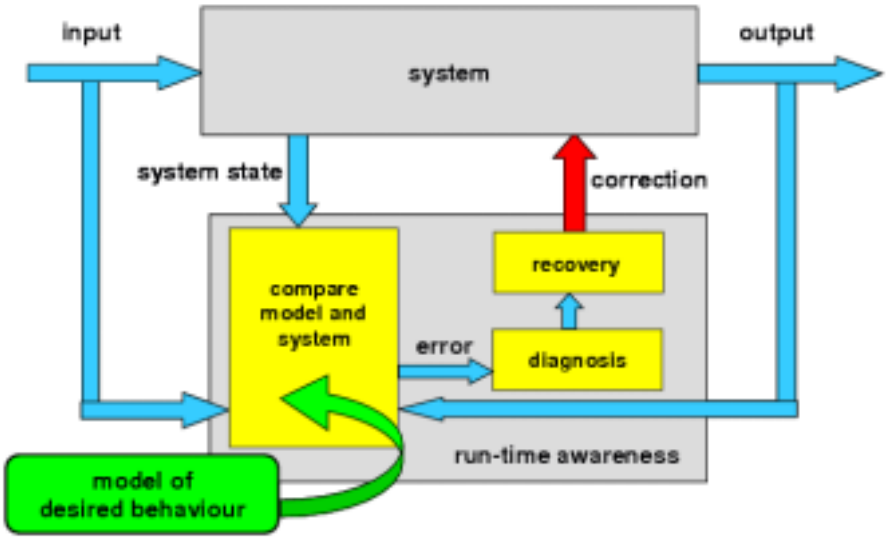

Figure 1: Adding awareness at run-time.

We discuss the main parts:

- *Observation:* observe relevant inputs, outputs and internal system states. For instance, for a TV we may want to observe key presses from the remote control, internal modes of components (dual/single screen, menu, mute/un-mute, etcetera), load of processors and buses, buffers, function calls to audio/video output, sound level, etcetera.
- *Error detection:* detect errors, based on observations of the system and a model of the desired system behaviour.
- *Diagnosis:* in case of an error, find the most likely cause of the error.
- *Recovery:* correct erroneous behaviour, based on the diagnosis results and information about the expected impact on the user.

We have implemented a general awareness framework in which an application and a model of its desired behaviour can be inserted.

This method, coupled to local recovery techniques, aims to minimize any user exposure to product-internal technical errors.

About the speaker: Jozef Hooman is a research fellow at the Embedded Systems Institute (ESI) since 2003. In addition, he is a senior lecturer in the group Model Based System Development at the Radboud University of Nijmegen since 1998. Before, he was a lecturer at the Eindhoven University of Technology, where he also received a PhD degree on a thesis entitled `Specification and Compositional Verification of Real-Time Systems'. His current research addresses various aspects of embedded systems, such as performance and reliability, the combination of formal methods and UML, and multi-disciplinary modelling.

Acknowledgement: This work has been carried out as part of the Trader project with NXP Semiconductors under the responsibility of the Embedded Systems Institute. This project is partially supported by the Dutch Ministry of Economic Affairs under the BSIK program.

1.2 Fault diagnosis of embedded systems

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Abstract: Fault diagnosis is the process of localizing the cause of systems failure. Automated fault diagnosis is emerging as an important factor in achieving an acceptable and competitive cost/dependability ratio for embedded systems.

In this presentation, we survey Model-Based Diagnosis (MBD) and Spectrum-based Fault Localization (SFL), two state-of-the-art approaches to fault diagnosis, that are aimed at diagnosing systems hardware and control software, respectively. We provide an overview of the field, and present recent MBD research results from the ESI-led Tangram project and the STW/PROGRESS-funded FINESSE project, and, most notably, recent SFL research results from the ESI-led Trader project.

About the speaker: Arjan J.C. van Gemund received a BSc in Physics, an MSc degree (cum laude) in Computer Science, and a PhD (cum laude), all from Delft University of Technology. He has held positions at the R & D organization of the Dutch multinational company DSM as an Embedded Systems Engineer, and at the Dutch TNO Research Organization as a High-Performance Computing Research Scientist. Currently, he is at the Electrical Engineering, Mathematics, and Computer Science Faculty of Delft University of Technology, serving as Full Professor. His current research interest is fault diagnosis of hardware and software systems. He has co-authored over 150 scientific papers.

Acknowledgements: Parts of this work have been carried out within (1) the Tangram project with ASML, (2) the Trader project with NXP, both under responsibility of the Embedded Systems Institute and supported by the Dutch Ministry of Economic Affairs under the TS and BSIK programs, respectively, and (3) within the FINESSE project, supported by the PROGRESS program of the Dutch Technology Foundation STW through grant DES.7015.

2.1 System-level control of warehouses

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Abstract: Warehouses are critical links in supply chains: they receive goods from many different suppliers, provide temporary storage of these goods, repack them, and distribute them to many different customers. It is not uncommon for a warehouse to deliver goods to different types of customers, such as shops and Internet customers. The way in which the goods are to be delivered to the various customer types differs. For instance, a shop customer may want its goods to be delivered in such a way that it can replenish its shelves in an efficient manner (i.e. similar products should be stored in the same container). On the other hand, an Internet customer wants to receive ordered goods via mail delivery.

A warehouse control system is responsible for controlling the warehouse operations needed to fulfil all customer requirements. Traditionally, warehouse control systems are centralized systems responsible for planning, scheduling, and execution of all warehouse operations. These operations include receiving, storage and retrieval, picking, consolidation, and shipping of goods. Besides these normal operations, a warehouse control system must also control the frequently occurring exceptions like equipment failure and data inconsistency. In fact, the large warehouse complexity makes it almost impossible to control all (normal and exceptional) operations in an optimal manner using a centralized warehouse control system.

An alternative to a centralized warehouse control system would be a fully decentralized warehouse control system. Such a system consists of a number of autonomous components, each controlling the operations in a limited part of the warehouse without any system-level coordination. It is however not clear whether a fully decentralized system is feasible: the desired system qualities, like performance and robustness, have to emerge from the individual qualities of the autonomous components.

The Falcon project, which was set up by the Embedded Systems Institute and Vanderlande Industries, investigates the feasibility of holonic warehouse control systems. These can be viewed as a hybrid form of fully centralized and fully decentralized control systems. The research involves the development of a framework that allows fast and simple experimentation with different holonic warehouse control systems [2].

The framework was inspired by the reference architecture PROSA for holonic manufacturing systems [3]. Like PROSA, our framework considers three types of (basic) holons: resource holons, logic holons, and order holons. These are similar to PROSA's basic holons, but they have been adapted to be more domain-independent, to allow application in the warehouse domain.

Following the holonic approach, warehouses can be seen as hierarchies of functional building blocks, each with unique responsibilities. This hierarchical structure is used to create a hierarchy of resource holons. For example, on the system level, resource holons are created for the functional areas for receiving, storage, picking, consolidation, and shipping. These areas each consist of a number of workstations that are also represented by resource holons.

The logic holons can be seen as a service directory: holons can register their services at a logic holon. Holons requiring a service to perform a task can consult a logic holon to obtain an overview of the holons that provide this service (and the corresponding costs). Because equipment may break down, holons can also unregister their services, making their services unavailable for other holons.

Order holons are created for the tasks to be performed in the warehouse. On the system level, these order holons correspond to customer orders. Customer orders are broken down into suborders to be performed by the warehouse's functional areas and workstations, resulting in a hierarchy of order holons.

Agent technology was used for the implementation of the holon framework: the framework was built upon JADE middleware [1]. JADE provides a means for holon lifecycle management, holon communication, and useful tooling. The framework was coupled to Vanderlande Industries' simulation environment, which provides a means to analyze a holon-controlled warehouse.

The framework uses a warehouse layout and a library containing reusable and parameterized behaviors as input. When the framework is started, it creates a hierarchy of resource and logic holons from the warehouse layout file. The layout file also specifies the behaviors of these holons. A hierarchy of order holons is created from a list of customer orders and the recursive decomposition of these customer orders into suborders.

Two experiments have been performed on an existing retail warehouse. The simulation experiments show that the framework provides a simple and flexible method to experiment with different holonic control strategies. Moreover, it helps Vanderlande Industries to determine the benefits of holonic warehouse control systems.

References:

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[2] Hristina Moneva, A Holonic Approach to Decentralized Warehouse Control, Eindhoven University of Technology, SAI Technical Report, August 2008.

[3] Hendrik Van Brussel, Jo Wyns, Paul Valckenaers, Luc Bongaerts, and Patrick Peeters, Reference Architecture for Holonic Manufacturing Systems: PROSA, Computers in Industry 37(3): 255-276, November 1998.

About the speaker: Jurjen Caarls received his M.Sc. degree in Applied Physics from the Faculty of Applied Sciences of the Delft University of Technology, the Netherlands. His M.Sc. thesis on `Fast and Accurate Robot Vision' for the RoboCup robots of the Dutch Soccer Robot team Clockwork Orange won the award of the best M.Sc. thesis of the Applied Sciences faculty in the year 2001. He is finishing a Ph.D. at the Quantitative Imaging Group of Delft University of Technology on camera pose estimation and sensor fusion for Augmented Reality, and is currently working on robust distributed warehouse control in the Falcon project.

Acknowledgement: This work has been carried out as a part of the Falcon project with Vanderlande Industries under the responsibility of the Embedded Systems Institute. This project is partially supported by the Dutch Ministry of Economic Affairs under the BSIK program.

2.2 Dependable robotic subsystem design for distribution centers

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Abstract: A distribution center (a warehouse) has as its main functionalities goods reception, goods storage, order picking, order consolidation, and order shipment. With respect to implementation, partly automated distribution centers are state of the practice. While fully automatic activities can be found in transport and in storage and retrieval functions, human activities mainly occur in order picking, where the variability of goods has the strongest impact on the implementation of the functions. However, humans become evermore a scarce and expensive resource for repetitive work in the distribution industry, whereas robotic technologies evolve to more versatile and cheaper solutions.

In the Falcon project, the challenge to design fully automated distribution centers is addressed. The main objective of the design process is to meet the customer's requirements with respect to costs, throughput, reliability, robustness, and scalability in the best possible way. The specific problem of designing fully automated DC's is to concurrently combine the design of the full system with the design of new robotic subsystems that must substitute the current human tasks. This inherently involves top-down and bottom-up reasoning that have to meet each other at the critical design issues.

We have confined the scope of the aforementioned design problem to a subsystem of coherent functions that comprise the current human functions and directly related functions. As a result of this confinement, our focus has been on item-related sub-functions: unpack cartons, singulate items, identity check, damage check, store items, transport items, and compose sub-orders. In this list, transport and storage are the sub-functions needed to decouple the other sub-functions in space and time.

Coming up with a new out-of-the-box system design, requiring the application of new technology in its subsystems, initially led to a developer's block: the system design should result in specs for the to be developed components, but also required specs of these components. The occurrence of either such a block in the design process or jumping to premature conclusions is rather common in such situations. A concurrent approach in the design space can avoid this. This approach consists of confronting top-down reasoning in the solution space with bottom-up elaboration of a couple of distinct solutions in that space. The different solutions from the bottom-up elaboration provide the necessary concreteness without collapsing the design space altogether.

In the top-down approach it is central to connect distribution center requirements, possible designs, and realization technologies through threads of reasoning, and subsequently select the most relevant and critical relationships in order to model them to gain insight. The relationships that we found from this approach, being the drivers for design decisions, are:

- Subsystem reliability in terms of correct function execution.
- Item variability related to specific technologies' capabilities.
- Subsystem performance in terms of function execution time.
- Subsystem cost versus its variability and multiplicity.

On their own, the models of these relationships are not sufficiently crisp to decide on the design of relevant subsystems to execute the item-related functions. These decisions heavily depend on the chosen technological solutions which do not exist yet. Therefore, this approach has to be augmented with the bottom-up direction.

In the Falcon project, the main relevant technologies for the studied subsystem which have to be addressed in the bottom-up approach are robot gripper design, robot arm design, and machine vision. The main issues to develop these components are closely related to the drivers from the top-down approach as well as the functions related to the subsystem of item handling:

- Defining grasp performance for compliant, underactuated grippers, which is a promising technology to obtain cheap grippers that can grasp a high variety of items.
- Designing adjustable, underactuated grippers to increase the ability to correctly and fast execute the required functions for a high variety of items.
- Fast machine vision algorithms that are able to discern one object from multiple identical objects.
- Increasing the robustness of machine vision algorithms against illumination variations.
- The suitable application of machine learning to ultimately feed the control of subsystem level actions.

The critical design issues that meet in both approaches can be readily recognized from the above listings. Robust performance and reliability of the subsystem at hand are both very relevant and critical in the context of fully automated distribution centers, while the technology to achieve this is not yet available in the required form. Therefore, we are commencing research in the directions of under-actuated, compliant hand design, new machine vision algorithms, and the development of new learning-to-see and learning-to-grasp control approaches, while modelling their effects on the above subsystem qualities that are critical for the system as a whole.

About the speaker: Roelof Hamberg received his master's degree in Physics from the University of Utrecht in 1987, and his PhD degree from the University of Leiden in 1991.

He worked from 1992 until 1998 at Philips Research in the field of perceptual image quality modelling and evaluation methods. From 1998 to 2001 he was developer of in-product control software at Océ. From 2001 to 2006 he was departmental manager at Océ, the first years in research, the last year in product development. As of October 2006 he is working as research fellow at ESI. Special area of interest is easy specification, exploration, simulation, and yet formal reasoning about system behaviour, the dynamic part of systems architecting.

Acknowledgement: This work has been carried out as a part of the Falcon project with Vanderlande Industries under the responsibility of the Embedded Systems Institute. This project is partially supported by the Dutch Ministry of Economic Affairs under the BSIK program.

3.1 Quasimodo

Quantitative System Properties in Model-Driven-Design of Embedded Systems

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Abstract: Characteristic for embedded systems is that they have to meet a multitude of quantitative constraints. These constraints involve the resources that a system may use (computation resources, power consumption, memory usage, communication bandwidth, costs, etcetera), assumptions about the environment in which it operates (arrival rates, hybrid behavior), and requirements on the services that the system has to provide (timing constraints, QoS, availability, fault tolerance, etcetera).

Model-Driven Development (MDD) is a new software development technique in which the primary software artifacts are models providing a collection of views. Existing MDD tools for real-time embedded systems are rather sophisticated in handling functional requirements but their treatment of quantitative constraints is still very limited. Hence MDD will not realize its full potential in the embedded systems area unless the ability to handle quantitative properties is drastically improved.

Quasimodo is an FP7 STREP project devoted to the develop theory, techniques and tool components for handling quantitative (e.g. real-time, hybrid and stochastic) constraints in model-driven development of real-time embedded systems.

The talk will give highlights of the results obtained so far within the project.

About the speaker: Kim Guldstrand Larsen is director of CISS, the Center for Embedded Software Systems and also director of DaNES, the Danish Network for Embedded Systems. He is also in the SG of the NoE ARTIST Design coordinating activities on modeling and validation. Dr. Larsen is member of the Royal Danish Academy of Sciences and Letters, Copenhagen, and is member of the Danish Academy of Technical Sciences.

In 1999, he became Honorary Doctor (Honoris causa) at Uppsala University, Sweden. In 2007 he became Knight of the Order of the Dannebrog. In 2007, he became Honorary Doctor (Honoris causa) at ENS Cachan, France. He has received Danish Citation Laureates Award (Thomson Scientific) as the most cited Danish Computer Scientist in the period 1990-2004. He has written one book, edited six books, and written 148 publications including 37 journal publications. He has co-authored six software-tools and is prime investigator of the tool UPPAAL.

3.2 Building dynamic information-centric systems-of-systems

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Abstract: The Poseidon project aims to discover new ways to build dynamic information-centric systems-of-systems. The Poseidon research statement is derived from the maritime safety and security domain of its carrying industrial partner Thales. Here, as in many other domains, future systems-of-systems will collaborate across former system boundaries in order to support decision making and situation awareness based upon a variety of heterogeneous information sources.

This talk provides an overview of the central aspects of the Poseidon project, e.g., situational awareness and visualization, recognition, and trustworthy information interoperability. We will focus in particular on runtime integration and acceptance for fast and flexible system-setup. The challenge is to gain flexibility, adaptability, and evolvability whilst retaining reliability, so that changes in a system-of-systems' configuration can be achieved in minimal time and with minimal effort while the system remains operational and reliable, even in the context of unforeseen events or scenarios.

The presented approach includes a platform and a methodology that integrate different techniques: process mining to determine a model of an unknown, existing system, adapter generation to glue systems into a system-of-systems, built-in compliance checking for runtime acceptance, and runtime health monitoring. Together they allow for non-obtrusive, built-in, runtime, and lightweight integration, testing, acceptance, and diagnosis.

About the speaker: Michael Borth graduated in Informatics at the University of Ulm (F.R.Germany) in 1999 with his thesis on 'The Generation of Bayesian Networks for the Diagnosis of Technical Systems' and joined DaimlerChrysler Research and Technology afterwards. Here, he worked on information mining for the analysis of complex systems, receiving his Ph.D. (Dr. rer. nat.) from the University of Ulm in 2004 for his work on 'Knowledge Discovery on Multitudes of Bayesian Networks'. Later on, as Senior Researcher, he focused on advanced concepts for E/E – architectures and architecture development, working in close cooperation with DaimlerChrysler Advanced Engineering and Mercedes-Benz Development, but also within international consortiums.

Michael Borth joined the Embedded Systems Institute in 2007. His work and research interests focus on information-centric architectures, systems of systems, embedded intelligence, and the role of uncertainty - both for the design of complex systems and the advanced information processing within such systems.

Acknowledgement: This work has been carried out as a part of the Poseidon project with Thales Nederland B.V. under the responsibility of the Embedded Systems Institute. This project is partially supported by the Dutch Ministry of Economic Affairs under the BSIK program.

4.1 Supervisory control synthesis for a patient support system

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Introduction: Present day complex systems are usually not designed from scratch. They are evolutions of previous generations of the system. Due to market demands and increasing competition, the number of features, and thus the complexity, of systems increases, while the time-to-market of a system should be decreased. At the same time, systems should meet high quality constraints. This necessitates the need for methods to maximize reuse and to minimize the effort to design new generations of a system.

In this research, the Model-Based Engineering (MBE) and the Supervisory Controller Synthesis (SCS) paradigms are used in the development process of a supervisory controller for a patient support table of a MRI scanner. The MBE paradigm facilitates model simulation and verification, as well as hardware-in-the-loop simulation early in the design process. In the SCS paradigm, the uncontrolled system and the control requirements are modeled. From these models, the supervisory controller is synthesized. The synthesized controller is correct by construction w.r.t. its control requirements and it is deadlock and livelock free. The SCS paradigm eliminates the time consuming and error-prone design step of the supervisory controller. Furthermore, if the required functionality changes, only the requirements need to be re-modeled. The combination of both paradigms increases the quality of the system and reduces its time-to-market.

Patient support case: In medical diagnoses, a Magnetic Resonance Imaging (MRI) scanner (see Figure 1) can be used to render pictures of the inside of a patient non-invasively. A MRI scanner consists of a bore that creates a strong magnetic field and a Patient Support System (PSS) that is used to position a patient inside the bore.

Fig.1 MRI scanner

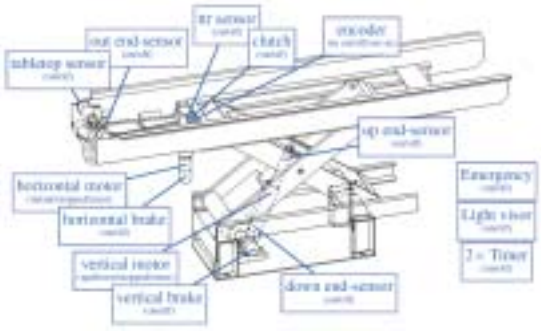

Fig.2 Patient support table

The patient support system consists of the patient support table, the local user-interface (PICU), and the light-visor. The patient support table (see Figure 2) can move vertically and horizontally. The vertical axis consists of a scissor lift with appropriate motor drive and end-sensors. The horizontal axis contains a removable tabletop which can be moved in and out the bore, either by hand or by a motor drive depending on the state of the clutch. It contains sensors to detect the presence of the tabletop, and the position of the tabletop. Finally, the system contains a light-visor to mark the scan plane, and an automated positioning system to position this scan plane in the center of the bore. The

system can either be controlled directly using the local user-interface (PICU), or remotely via the MRI control system.

In this research, a subset of the functionality of the patient support system is modeled. The emergency system, the light-visor with automated positioning, and the remote control system are not discussed here. The model of the uncontrolled PSS consists of 17 small automata describing the horizontal axis, the vertical axis, and the user interface buttons. The uncontrolled system consists of 1296 states and 27360 transitions between them. The model of the control requirements consists of 16 small automata. Some examples of modeled control requirements are:

- Do not move beyond end sensors.
- Only motorized movement if clutch is active.
- No motorized movement if Table-Top-Release sensor is active.
- Only move vertically if horizontally in maximally out position.
- Tumble switch moves table up and down, or in and out.

Using the model of the uncontrolled system and the model of the control requirements, a supervisory controller has been sythesized. The computation of the supervisor takes only a minute on a desktop pc. This supervisor consists of 2816 states and 21672 transitions. The synthesized supervisor has been simulated in parallel with the (hybrid) model of the plant. The synthesized supervisor has also been simulated in real-time with the actual patient support system (hardware-in-the-loop simulation).

About the speaker: Rolf Theunissen received his M.Sc. degree Mechanical Engineering from the Eindhoven University of Technology in July 2006. During his master program, he focused on process algebraic linearization of the hybrid Chi formalism. Currently, he participates in the Darwin project, which aims to provide generic methods for the design of highly evolvable systems. He is a member of the (Dutch) Institute for Programming research and Algorithmics (IPA).

Acknowledgement: This work has been carried out as a part of the Darwin project with Philips Healthcare Nederland under the responsibility of the Embedded Systems Institute. This project is partially supported by the Dutch Ministry of Economic Affairs under the BSIK program.

4.2 The value of investments in evolvability

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Problem statement: Software architecture is an established practice to guide the system design decisions towards fulfilling requirements on various quality attributes. The value of investments in quality attribute such as modifiability or evolvability is not directly observable by users and their benefits to the developing organizations are difficult to quantify. This poses a challenge how to explain and estimate the value of investments in evolvability to support such architectural investment decisions.

Framework: Evolvability is the ability of a system to adapt to changing requirements with predictable, minimal effort and time. Investment in evolvability gives a possibility to decide on a shorter term to develop features when the new feature is requested, with shorter time-to-market and reduced development effort. We propose a framework to estimate the value of investment in evolvable architecture based on an economic Real Options approach.

Evolvable architecture has a threefold benefit. First, it reduces the risk of implementing features upfront that turn out later to be undesirable. Second, it increases revenue implementing the requested features with shorter time-to-market and reduced cost. Third, it will create opportunity to implement features that otherwise would be too costly to implement on the current architecture. Figure 1 shows a decision tree for evaluating the investment in evolvability with two investment decisions. First, a decision to invest in architecture implementation (buying the option). Second, a decision to invest in deploying the architecture (exercising the option), which involves developing new features, installing the software on systems, or offering new services. The architecture investment will pay off when the present value of the cash flow facilitated by the evolvable (new) architecture is greater than the cash flow facilitated keeping the existing (old) architecture.

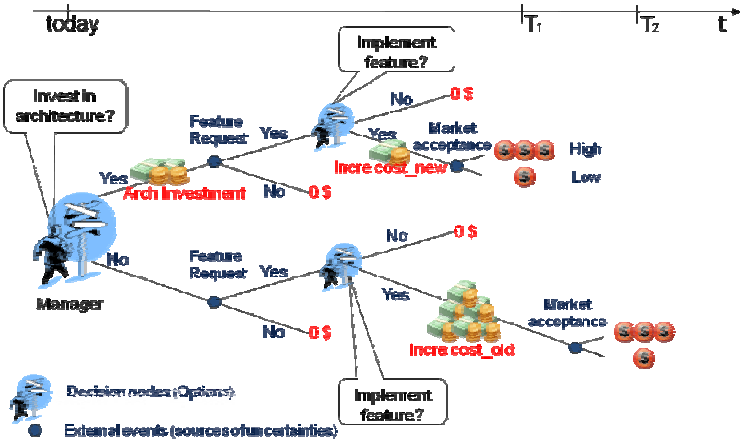

Figure 1. A decision tree of architectural investment

We identify four parameters to estimate the value of investment in architecture: cost, time, market value, and uncertainty.

- **Cost.** Architectural Investment, Arch Invest. Cost of developing an individual feature, Development cost. Cost of overall maintenance of the system, Maintenance cost. The last two costs will be different in scenarios with the existing and the new architecture. Table 1 shows the cost savings of investment in architecture.

- **Time.** Implementation time will define the moment to start architecture and Deployment time defines how long we may take the benefits of the architecture. Time to market is the time until the architecture is deployed to generate new cash flow.
- **Market value.** The market value is the difference in the market value of the feature deployed on the existing and the new architecture with respect to time-to-market, Δ Market Value.

	New Architecture	Existing Architecture	Cost Savings
Maintenance Cost	Maint Cost new	Maint Cost old	Δ Maint Cost
Development cost	Dev Cost new	Dev Cost old	Δ Dev Cost

Table 1. Cost savings

- **Uncertainty.** The probability of the feature request and market acceptance.

Case study: We estimated the economic value of the investment in phasing out legacy software in a medical imaging system in Philips Healthcare. The legacy software is tightly coupled with the rest of the software system. The legacy software is used rarely but its functionality is still requested by the customer. Any change request has to be implemented and tested in legacy and the rest of the software. The developers experience high maintenance cost, double test effort, and low extensibility. Phasing out legacy will keep all functionality of the system during and after the phase-out project. The investment and the duration of the phase-out project are Arch Investment = 24 man-years and Implementation time=4 years. We were asked to valuate this investment retrospectively.

To estimate parameters in Table 1, we interviewed relevant stakeholders and investigated the time-keeping archive of software developer's efforts with the following findings. Deployment time = 5 years is based on the roadmaps of the organization. Legacy code is removed, Maint new = 0. The stakeholders could not foresee any new features, Market Value = 0. Without new features envisioned, Δ Dev Cost = 0. The maintenance effort of legacy software, Maint_old = 0.1-1 fte. The maintenance cost of keeping the legacy software itself is not so high, because the legacy code is very stable. The results were surprising low and could not justify the large up-front investment, so we had to investigate further.

We interviewed several architects involved in different development projects that have to be integrated with the legacy software. The new development projects have to keep their software compatible with the legacy, slowing down development and increasing their development effort. This effort of problem solving with the legacy is administrated in the time-archive as development effort. Architects estimated the cost savings of 36-40 man-years in the new development projects because they do not have to integrate with the legacy during the four years phase-out project. Investment in phasing out of IA = 24 man-years was justified. In this case the pay-off of the phase-out investment has already started before the end of the project, because new developments can often afford to be incompatible with the phased-out software, since they will be released after the phase-out is completed. The investment in evolvability brings benefits not on the system level (reducing maintenance cost) rather on the organizational level (cross-project benefits).

The data collection to apply this framework is not trivial. Finding and understanding the value of the architectural investments require good knowledge of the organization and interviewing the right people. The framework establishes a new way of thinking to support decisions in architectural investments on an economic basis in industrial practice.

About the speaker: Ana Ivanovic is a research scientist at the Healthcare Systems Architecture group at Philips Research in The Netherlands. She is pursuing her PhD work on architectural decisions making on an economic basis. Her research interests include value-based engineering, healthcare technology assessments, and decision making. She received her MSc in Electrical Engineering from Belgrade University.

Acknowledgement: This work has been carried out as a part of the Darwin project at Philips Healthcare Nederland under the responsibility of the Embedded Systems Institute. This project is partially supported by the Dutch Ministry of Economic Affairs under the BSIK program.

4.3 Top-down generation of execution architecture views of large embedded systems

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Abstract: The execution architecture of a system maps its functional decomposition on the run-time structures that determine its real-time and performance behavior, which includes issues such as communication, concurrency, scheduling, synchronization, mutual exclusion, and priorities among its components [2]. Often in organizations developing large embedded systems, architects and designers require execution architecture information to formulate and eventually answer questions about the run-time issues and characteristics of a system and its components. For instance, when following a multi-view architecting method like CAFCR [1, 2], an execution architecture view contributes to describe the technology mapping of the system: show which software and hardware technologies is used to realize the various parts of the system in a conceptual architecture. In general, execution architecture information will often be useful to analyze the feasibility and impact of change and maintenance activities, especially when change and maintenance activities aim to improve the existing run-time structures and manage unpredictable system behavior.

Even if an execution architecture is constructed and used within the system design process, when the system implementation has started or the system has changed (more than once), it tends to be frozen into static documents that progressively become inaccessible and lose their value. This situation is a problem especially in organizations developing large and complex embedded systems (i.e. implemented with different programming languages and off-the-shelf components). To address this problem, we present a method to construct and maintain execution architecture views of large and complex embedded systems. This method is an iterative and problem driven approach that follows a top-down strategy to help software architects and designers to describe and decompose a complex system into high-level abstractions such as execution scenarios and software components. In addition, the high-level abstractions are respectively mapped to actual runtime processes taking into account implementation artefacts, hardware, and platform resources. Figure 1 illustrates the presented method together with our execution meta-model: a conceptual organization of abstractions that build the execution of a software system.

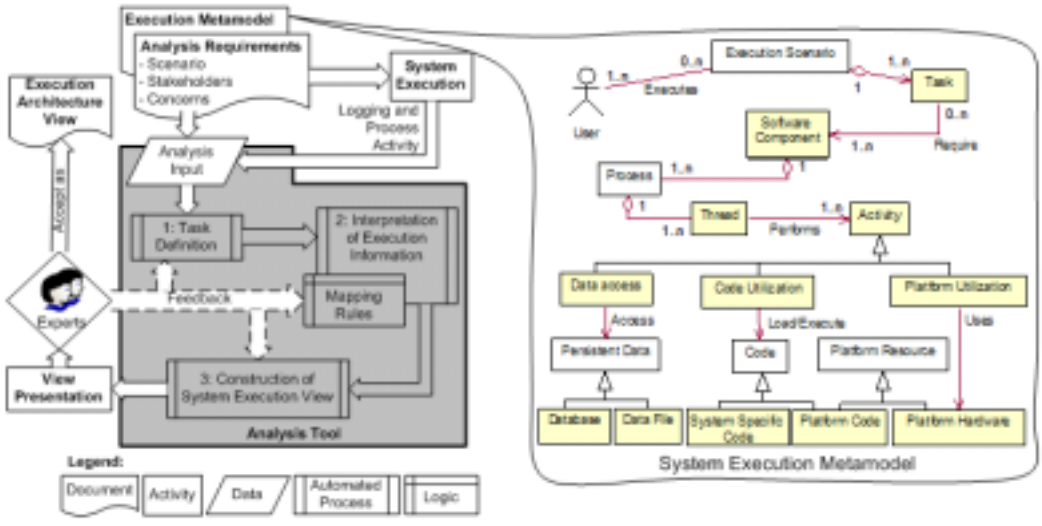

Figure 1. Top-down Generation of Execution Architecture Views

The current execution architecture views that our method constructs are scenario views: graph-based overviews, matrices, and sequence diagrams. Together, these views aim to provide navigability from overview to detailed information and support the analysis of the execution architecture of a complex system in a top-down fashion. In practice, this method can be applied regardless of the system's

implementation technology. However, it requires system logging infrastructure and monitoring facilities on the running platform. These factors facilitate the gathering of up-to-date execution data without interfering significantly with the actual run-time structure and properties of the system. In addition, the application of this method may demand several iterations to generate the required views that identify the concerns or problems of a change or maintenance activity. This is required because at the early stage of an analysis process, runtime concerns are either unknown or ill-defined. Figure 2 shows examples of execution architecture views constructed in the application of this method to analyze the software of the MRI system developed by Philips Healthcare.

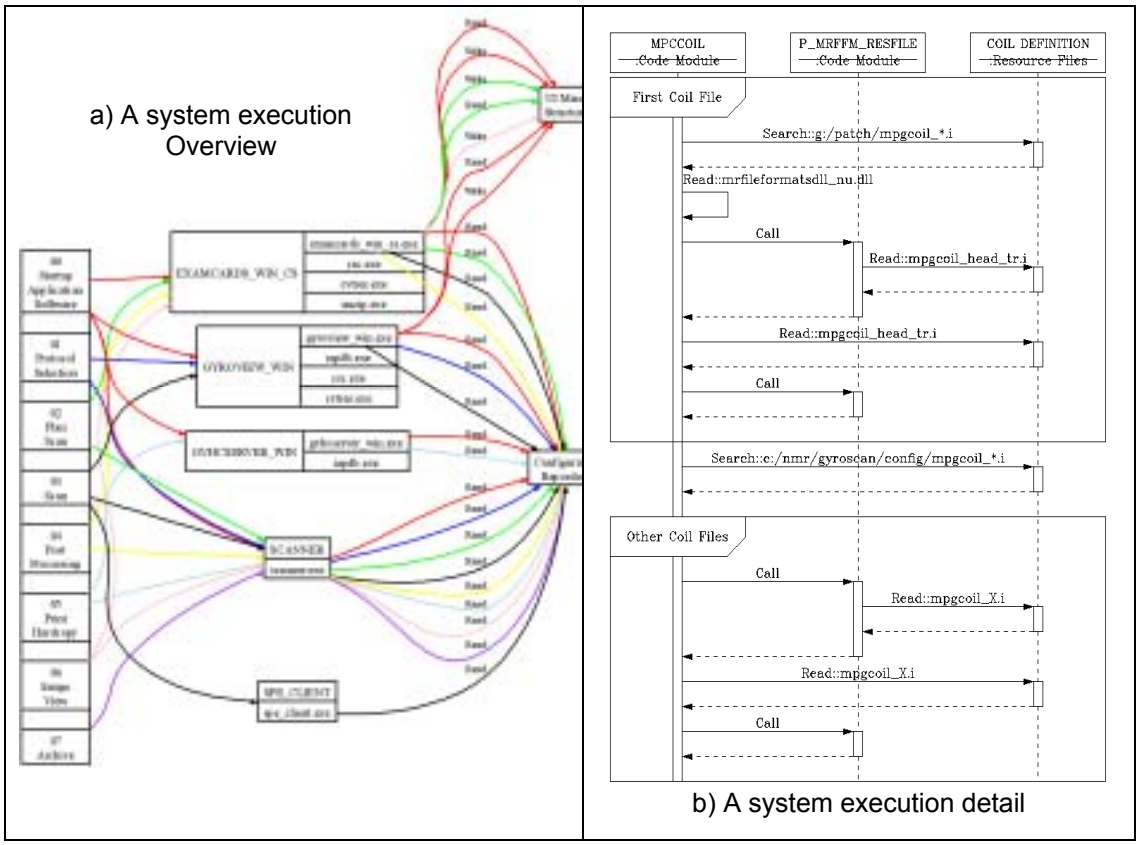

Figure 2. Execution Architecture Views of the Philips MRI System

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About the speaker: Pierre America received a Master's degree from the University of Utrecht in 1982 and a Ph.D. from the Free University of Amsterdam in 1989. He joined Philips Research in 1982 where he has been working in different areas of computer science, ranging from formal aspects of parallel object-oriented programming to music processing. During the last years he has been working on software and system architecting approaches for product families. He has been applying and validating these approaches in close cooperation with Philips Medical Systems. Starting in 2008 he is working part of his time as a Research Fellow at the Embedded Systems Institute, where his main focus is on evolvability.

Acknowledgement: This work has been carried out as a part of the Darwin project with Philips Healthcare Nederland under the responsibility of the Embedded Systems Institute. This project is partially supported by the Dutch Ministry of Economic Affairs under the BSIK program.

5.1 Introduction to the 3TU dependability track

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Abstract: In 2002, the three Dutch technical universities (Delft, Eindhoven, and Twente: 3TU) were among the founders of the Embedded Systems Institute. Since then, these three universities have intensified their way of collaboration, leading to the creation of several centers of excellence, including the Center for Dependable ICT Systems (CeDICT).

We briefly introduce the CeDICT, the anticipated collaboration between ESI and CeDICT, and the six new full professors that have been appointed within CeDICT, after which two of them will take over and present their latest results in the area of dependability for embedded systems.

About the speaker: Arie van Deursen is a professor in Software Engineering at Delft University of Technology, and a member of the CeDICT management team. His research interests include software evolution, software testing, and model-driven engineering.

5.2 Dependable railway infrastructure

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Abstract: I will describe the plans in the recently started FP7 project INESS, Integrated European Signaling System. The coordinator is UIC (International Union of Railways). Participants are national railway operators of several countries, and manufacturers, like Siemens. Dutch participants of INESS are the railway operator ProRail, and the academic institutes TU Eindhoven and U Twente, supported by LaQuSo.

The overall goal of INESS is to develop harmonized, standardized and validated specifications for the new generation of European interlocking systems. To this end, the European Railway Traffic Management System (ERTMS) is being developed. The first advantage of harmonized requirements is the interoperability of systems between different countries. The second advantage is that it increases the competition between manufacturers.

Besides standardization, ERTMS also provides new functionality. Basically, the higher ERMTS levels move functionality from the railway infrastructure into the train, while communication is provided by wireless networks (GSM).

Obviously, railway-signaling systems are safety critical. A so-called interlocking regulates the control of points and signals, in order to prevent collisions among trains, and between trains and other traffic. As a consequence, there are strict safety requirements, and strict certification procedures, laid down in CENELEC standards.

The academic partners will play an important role in formalizing the requirements, modeling the signaling systems, and validating the specification. We expect to contribute to the automation of the testing and certification process. To this end, we will use and develop tools to formally prove that signaling systems meet their safety requirements. The methodology and tools of mCRL2, augmented with automated provers (SAT solvers) are expected to play a key role.

We view this project as an excellent example of 3TU collaboration in CeDICT, on a system with high dependability demands, and a strong societal relevance and visibility.

About the speaker: Jaco van de Pol is full professor of the Formal Methods and Tools group in the Computer Science Department at the University of Twente. This is one of the new CeDICT chairs in 3TU.NIRICT, the Center on Dependable ICT systems. His research interest is validation of concurrent and embedded systems, by means of model checking, theorem proving and testing. His interest is in the development of new theories, new tools, and application to industrial systems. His recent research is on distributed and multi-core implementation of model checkers.

5.3 Securing information in systems of systems

Security in Poseidon

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Abstract: The Poseidon project is about situational awareness in a System of Systems (SoS), applied to the domain of Maritime Safety and Security (MSS, e.g. coast surveillance). The project's challenge is to develop a flexible, adaptable, and evolvable SoS, where sensitive information needs to be shared among the participating entities. Security challenges include protection of sensitive data from unauthorized disclosure, using content- and context-aware security policies, secure interaction between (possibly untrusted) members of dynamic coalitions, inter-operability of heterogeneous policies using ontology-based reasoning, tuning local policies to ensure global security.

About the speaker: Sandro Etalle (1965) graduated cum laude in Mathematics at the University of Padova in 1991. He carried out his PhD research partly at the University of Padova under the supervision of Annalisa Bossi and mostly at the CWI (Centrum voor Wiskunde en Informatica) under the supervision of Krzysztof Apt. In 1995 he gained his PhD in Computer Science from the University of Amsterdam. He worked for the Universities of Amsterdam, Genova and Maastricht before joining the University of Twente in 2001. After a period visiting the University of Trento, he now leads the Security group at the TU/e, and works for the University of Twente one day a week. Sandro Etalle started researching the verification of security protocols in 2001. Since then, his main research focus has been policy enforcement and the protection of confidential data. Currently, his interests include intrusion detection and risk management.

Acknowledgement: This work has been carried out as a part of the Poseidon project with Thales Nederland B.V. under the responsibility of the Embedded Systems Institute. This project is partially supported by the Dutch Ministry of Economic Affairs under the BSIK program.

6.1 Performance model generation for MPSoCs with resource management

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Abstract: Multi-processor system-on-chip (MPSoC) design is profiting considerably from the trend towards model-driven design. Design choices in this area cover considerations on alternative parallelisations of application software, alternative architectures for the hardware platform and different ways to map applications onto the platform. Various paradigms exist for modeling applications and also for modeling platforms.

This presentation discusses a tool for generating abstract performance models of MPSoC systems with resource management to further automate their design-space exploration.

The tool supports several traditional paradigms for specifying applications and uses a new model of architecture to enable describing hardware platforms at a much higher abstraction level than traditional hardware description languages. The tool relies on a collection of so-called modeling patterns to convert application and platform specifications together with a mapping into one unifying model expressed in a formal general-purpose modeling language that offers extensive support for performance analysis.

About the speaker: Bart Theelen received his Master's degree in Information Technology in 1999 and his Ph.D. in 2004 from Eindhoven University of Technology. Until recently, he was a postdoc at the Department of Electrical Engineering of the Eindhoven University of Technology, working on performance modeling and performance analysis in the context of system-level design. His research interests include modeling methods, formalisms and techniques for the design, specification, analysis and synthesis of hardware/software systems.

6.2 Daedalus: towards composable multimedia MP-SoC design

An integrated framework for system-level exploration, synthesis, programming and prototyping of MP-SoCs

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Abstract: The complexity of modern embedded systems, which are increasingly based on MultiProcessor-SoC (MP-SoC) architectures, has led to the emergence of system-level design. To cope with the design complexity, system-level design aims at raising the abstraction level of the design process. Key enablers to this end are, for example, the use of architectural platforms to facilitate re-use of IP components and the notion of high-level system modeling and simulation. System-level design for MP-SoC-based embedded systems however still involves a substantial number of challenging design tasks. For example, applications need to be decomposed into parallel specifications so that they can be mapped onto an MP-SoC architecture. Subsequently, applications need to be partitioned into HW and SW parts since MP-SoC architectures often are heterogeneous in nature. To this end, MP-SoC platform architectures need to be modeled and simulated to study system behavior and to evaluate a variety of different design options. Once a good candidate architecture has been found, it needs to be synthesized, which involves the synthesis of its architectural components as well as the mapping of applications onto the architecture. To accomplish all of these tasks, a range of different tools and tool-flows is often needed, potentially leaving designers with all kinds of interoperability problems. Moreover, there typically remains a large gap between the deployed system-level specifications (or models) and actual implementations of the system under study, known as the implementation gap. Currently, there exist no mature methodologies, techniques, and tools to effectively and efficiently convert system-level MP-SoC specifications to RTL specifications.

Recently, we presented our Daedalus system-level design framework, which addresses the above design challenges. The entire Daedalus framework has been developed as high-quality software distributed under Open Source licenses. Daedalus' main objective is to bridge the aforementioned implementation gap for the design of multimedia MP-SoCs. It does so by providing an integrated and highly-automated environment for system-level architectural exploration, system-level synthesis, programming, and prototyping. The Daedalus design flow, which leads the designer from a sequential application to an MP-SoC system implementation on an FPGA with a parallelized application mapped onto it, can be traversed in only a matter of hours. Evidently, this offers great potentials for quickly experimenting with different MP-SoCs and exploring design options during the early stages of design.

In this presentation, we report on our first deployment experiences with the Daedalus framework. Daedalus is currently being deployed in a project together with the Dutch SME Chess B.V., which involves the design of an image compression system for very high-resolution (in the order of Gigapixels) cameras targeting medical appliances. In this project, the Daedalus framework is used for design space exploration (DSE), both at the level of simulations and prototypes, in order to rapidly gain detailed insight on the system performance. To this end, we present initial results from a DSE

study we performed with a JPEG encoder application, which exploits both task and data parallelism and which is mapped onto a range of different MP-SoC architectures.

About the speaker: Andy Pimentel is associate professor in the Computer Systems Architecture group of the Informatics Institute at the University of Amsterdam. He holds the MSc and PhD degrees in computer science, both from the University of Amsterdam. He is co-founder of the International Symposium on embedded computer Systems: Architectures, Modeling, and Simulation (SAMOS) and is member of the European Network of Excellence on High-Performance Embedded Architecture and Compilation (HiPEAC). His research focus is on the study and development of efficient and effective methods, techniques and tools that aid computer designers in the design process, especially during the early stages of design. In more general terms, his research interests include computer architecture, computer architecture modeling and simulation, system-level design, design space exploration, performance and power analysis, embedded systems, and parallel computing. He serves on the editorial boards of Elsevier's Simulation Modeling Practice and Theory as well as Springer's Journal of Signal Processing Systems. Moreover, he also serves on organizational committees for a range of leading conferences and workshops, such as the SAMOS Symposium (Board member), DATE (PC member), IEEE ICCD (PC member), FPL (Local Organization Chair in '07, PC member) and IEEE ESTIMedia (PC Chair). Andy Pimentel is senior member of the IEEE and member of the IEEE Computer Society.

Acknowledgement: This work has been carried out as a part of the Artemisia and Daedalus projects (with NXP and Chess). This research is supported by PROGRESS, the embedded systems research programme of the Dutch organization for Scientific Research NWO, the Dutch Ministry of Economic Affairs and the Technology Foundation STW.

7.1 Decomposing software architecture to introduce local recovery

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Abstract: Local recovery is an effective fault-tolerance technique to attain high system availability. For achieving local recovery the architecture needs to be decomposed into separate units that can be recovered in isolation. There are usually many decomposition alternatives to consider, where each alternative may perform different with respect to availability and performance metrics. Moreover, introducing local recovery to a software system, while maintaining the desired functionality, is not trivial and requires a substantial development and maintenance effort.

We propose a systematic approach for decomposing software architecture to introduce local recovery. Our approach enables the following: 1) modeling the design space of the possible decomposition alternatives, 2) reducing the design space with respect to domain and stakeholder constraints, 3) making the desired trade-off between availability and performance metrics, and 4) reducing the effort, while decomposing software architecture for the implementation of local recovery. To support the approach, we have developed a set of analysis tools and a framework.

We discuss our experiences in the application and evaluation of the approach for introducing local recovery to the open-source media player called MPlayer.

About the speaker: Hasan Sozer is a PhD student at the University of Twente, The Netherlands. He received the BS and MS degrees in computer engineering from Bilkent University, Turkey, in 2002 and 2004, respectively. From August 2002 until January 2005, he worked as a software engineer at Aselsan Inc. in Turkey. His research interests include software engineering and wireless ad hoc networks.

Acknowledgement: This work has been carried out as a part of the Trader project with NXP Semiconductors under the responsibility of the Embedded Systems Institute. This project is partially supported by the Dutch Ministry of Economic Affairs under the BSIK program.

7.2 Measurement and analysis of user perception of picture quality failures in LCD TVs

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Abstract: Innovative Consumer Electronics (CE) products, such as LCD televisions, are becoming increasingly complex, both in terms of the product architecture (i.e. increasing software content, ambient technologies, and open systems) [1] as well as in terms of the number of functionalities provided [2]. For example, the LCD television of today can be used to access the Internet, watch digital photos, and connect to a personal computer to watch downloaded movie content. Furthermore, because of the globalization of demand, these products require a high level of connectivity with other products and other brands in very different configurations. Research by Den Ouden [3] has shown that an increasing number of consumer complaints and product returns for such products is reported. Because consumers do not always understand how these complex products are structured [4], they often perceive the product's (mal-)functioning differently than designers do. Even when a product is still functioning according to technical specifications, a consumer might think otherwise. To prevent such product failures in the field, there is a need to incorporate more consumer focus in the new product development process [3]. Specifically, it is necessary for the designers to have more insight into how consumers perceive potential product failures, to support critical design decisions early in the product development process.

This research focuses on the analysis and measurement of how consumers perceive picture quality failures in innovative LCD televisions. Television picture quality can be influenced by internal problems in the TV (e.g. faults in the software) when processing or displaying the TV signal, as well as by external problems outside the TV such as bad weather or cable connection problems [5]. Problems internal to the TV could, for example, result in ghosting or blocking artifacts. Bad weather or cable connection problems could, for example, result in noise on the screen. Because consumers might attribute externally caused problems to the TV system or the other way around, it is important for product developers to gain insight into how consumers perceive these different types of failures in picture quality. These insights can be used to prioritize product failures and software quality aspects from a consumer perspective.

To investigate the influence of different types of failures on failure perception, two failure scenarios (i.e. one scenario with noise due to a bad cable signal and one scenario with blocking artifacts due to faults in the software) were designed in close collaboration with digital TV system experts [5]. The user's perception of those failures was evaluated in a carefully designed experiment with 40 subjects in a between-subjects design. The dependent variables measured included failure perception, perceived failure impact (i.e. the percentage loss of functionality [6]) and failure attribution (i.e. the perceived cause of the failure). Further research includes the evaluation of various failure scenarios in a large-scale web-based survey and experiments combined with an investigation of the influence of the user characteristic 'consumer knowledge' on the failure perception variables to gain insight into how different consumers perceive complex product failures.

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About the speaker: Jeroen Keijzers received his BSc degree and MSc degree (with honors) in Industrial Engineering and Management Science from Eindhoven University of Technology. His MSc thesis, resulting from an internship at Philips Applied Technologies, was in the field of quality and reliability engineering. This research investigated how consumer test strategies should be defined to identify relevant user-perceived product failures in innovative consumer electronics products early during the product development process.

His current Ph.D. research at the Business Process Design group at the Faculty of Industrial Design, Eindhoven University of Technology, investigates how consumers perceive product failures. More specifically, he investigates how a specific user characteristic, consumer knowledge, influences use actions and attribution of product failures in innovative consumer electronics products.

Acknowledgement: This work has been carried out as a part of the Trader project with NXP Semiconductors under the responsibility of the Embedded Systems Institute. This project is partially supported by the Dutch Ministry of Economic Affairs under the BSIK program.

8.1 Diagnosis of wafer stage failures

Model Based Diagnosis in practice

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Abstract: The wafer scanners of ASML are on the leading edge of technology. Time to market dictates that hundreds of engineers work in parallel on the development of these systems. To avoid delaying the first shipment, the development of diagnostic facilities should go hand-in-hand with development of the subsystem-to-be-diagnosed. One approach is to base these facilities on existing models of the subsystems.

Model Based Diagnostics (MBD) is a methodology that uses a model as the basis for diagnostics. A model of a system is fed into a reasoning engine, and using actual inputs and outputs the reasoning engine determines which part(s) of the system failed.

The Tangram project introduced model based diagnostics at ASML. In cooperation with Tangram, a pilot project was started to create diagnostic tooling for the wafer stage subsystem. The project concentrated both on converting the wafer stage models, and on the integration of the MBD tooling into the existing toolset of the service engineers.

The presentation will show the results of the MBD approach in ASML and discuss the lessons learned during the project.

About the speaker: Christian Bakker (1969) has a degree in Computer Science from Delft University and participated in the Software Technology postgraduate program at Eindhoven University.

At ASML he has worked as a software architect in the development of infrastructure for diagnostics and diagnostic tooling.

Acknowledgement: This work has been carried out as a part of the Tangram project with ASML under the responsibility of the Embedded Systems Institute. This project is partially supported by the Dutch Ministry of Economic Affairs under the TS program (grant TSIT2026).

8.2 Introducing WeaveC at ASML

Valorisation in practice

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Abstract: The Ideals project was started based on the analysis that the required SW engineering effort and lead time to deliver new functionality at ASML was becoming too long. An important reason that was identified was that, in addition to new functionality, all so-called cross-cutting concerns such as error handling, diagnostics information creation and function tracing, have to be implemented and tested each time as well. The research project focused on how to minimize this part of the engineering effort.

During the research project a number of potentially valuable methods, technologies and tools were invented and created. During the project we have succeeded in integrating one of these ideas in the engineering flow at ASML: a tool called WeaveC that is capable of supporting aspect oriented programming on the C codebase from ASML. This transfer was done by ASML, in close co-operation with the research project.

The presentation will discuss the process followed to get ASML to adopt the research results and present the results that ASML has achieved with the WeaveC technology. It will give a short introduction in the nature of the technology itself, but the main focus is on the way it was introduced at ASML.

About the speaker: Remco van Engelen (1971) has a degree in Computer Science from Eindhoven University. At ASML he has worked as a software designer and a software architect in the development of metrology and motion control software. He initiated and participated in the Ideals research project and is now responsible for the software development infrastructure within ASML.

Acknowledgement: This work has been carried out as a part of the Ideals project with ASML under the responsibility of the Embedded Systems Institute. This project is partially supported by the Dutch Ministry of Economic Affairs under the TS program (grant TSIT3003).

9.1 Featherlight collaborative ambient systems

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Abstract: In the Featherlight project, we investigate new light weight distributed mechanisms for networking and distributed collaboration. These mechanisms can operate in a challenging environment of self-organizing collaborative ambient systems, where nodes move, fail, and energy is a scarce resource. In this project, we develop new featherlight protocols, algorithms, and firmware for networking and distributed collaboration as a basis for building self-organizing, dependable and collaborative ambient systems. We evaluate their feasibility through both theoretical analysis and experimentation in order to keep the gap to further industrial development as small as possible.

One of the issues we considered was regarding the architecture of the software inside the sensor nodes. We built our applications on top of a dynamic architecture where the software modules could be loaded/unloaded at run time based on the dynamics of the environment and the tasks to be performed. These software modules communicate with each others via a publish/subscribe server, thus allowing easy reconfigurations and dynamic data flows inside the nodes. The next step was extending the architecture past the single device, by combining the publish/subscribe servers of several nodes over a virtual communication channel. Software components in a node could access data being created on different nodes in a transparent manner. The challenges referred to maintaining this virtual communication channel available despite the mobility of devices, unreliable radio communication, etcetera. Several distributed algorithms have been developed for creating and maintaining this virtual channel and were evaluated both theoretically and in real world implementations.

Another aspect related to the software architecture running inside the sensor nodes is the interfacing to the software modules running inside the devices. We came up with a unified approach of accessing every software module, allowing full flexibility for the functionality present in the devices. The interface makes use of a set of general purpose functions (as enable/disable, report status, report version number, etcetera) and a set of module specific functions to be supplied by the users. The parameters and return results are offered in a standardized form. This allows the networking protocols to ignore the format of the transferred data and become truly general purpose. The standardized interface is flexible enough to allow easy integration with existing software infrastructure with little or no modifications done to the infrastructure.

On top of the dynamic software architecture, we developed a service discovery protocol that runs within the wireless sensor network. Using this protocol, sensor nodes have the possibility to discover and use the services offered by other nodes in the network, or external users can discover and use the services available in the wireless sensor network. The sensor network self-organizes in a clustered structure that acts as a distributed directory of service registrations. The clustering offers the necessary support to achieve energy-efficient discovery within the network, by organizing the clusterhead nodes to form a distributed service registry. A service lookup results in visiting only the clusterhead nodes. To minimize the communication costs during discovery of services and maintenance of a functional distributed service registry, we propose a clustering algorithm which makes decisions based on one-hop neighborhood information and constructs a set of sparsely distributed clusterheads. The clustering algorithm, together with the service discovery protocol, are both theoretically and practically evaluated.

About the speaker: Stefan Dulman received his engineer degree in telecommunications from `Gh. Asachi' Technical University of Iasi (Romania) in 2001 and his master degree from the same university in 2002. He received a PhD degree in computer science from University of Twente in 2005. He is currently employed as a postdoc researcher in the Pervasive Systems group at the University of Twente and a part time researcher at Ambient Systems BV. His current research interests are in the field of embedded systems, with a special focus on wireless sensor networks.

9.2 ViewCorrect: embedded control software design using a model-driven method

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Abstract: This presentation shows a model-based, iterative approach for designing embedded control software for mechatronic applications.

The components for a mechatronic system are made by engineers from different disciplines, each having their own way of working and tooling. Also, the dynamic behavior of the mechanics (i.e. machine to be controlled) must be taken into account when designing the embedded software, because this dynamic behavior determines besides the functionality of the control actions also the timing constraints and time-dependent behavior of the software.

It is hard to test the complete mechatronics design during the development phase; often only the individual parts or components can be tested separately. When the entire system is finally integrated and tested, unforeseen problems arise. It is often at the boundaries of the disciplines that mistakes are made: incorrect gear ratios, mistaken polarity of a motor or software connections mapped by hand. Furthermore, the time budget left for software development decreases often when system complexity, and thus software complexity, increases.

The presented model-based approach allows for integration of discipline-specific parts on the model level (during design phases) instead of on the code level (during realization and test phases).

The design work is conducted as a stepwise refinement process, using simulation (i.e. model execution) as means of testing on all levels in the design process, formal verification of the software and automatic generation of embedded software. It consists of four major steps: (1) dynamic behavior modeling of the machine; (2) control law design; (3) embedded (control) software design; (4) embedded software realization. In this contribution, the focus is on the last 2 steps. In each step a stepwise refinement approach is used to design the system components.

The design method is demonstrated by presenting the whole design trajectory using a newly designed demonstration setup, a Cartesian plotter. To insure first-time right deployment on-target of the plotter software, the software was tested first in a virtual prototype. Besides formal verification via FDR2 and tests with simple test-benches, the dynamic systems model of step 1 is re-used in a co-simulation experiment together with the software. The transition from virtual prototype to target implementation is done by replacing only the co-simulation interfaces with real-I/O. The resulting target implementation is first-time right.

About the speaker: Marcel Groothuis (MSc 2004) is PhD candidate at the Control Engineering group of the department of EE-M-CS of the University of Twente. His research project is the STW/PROGRESS funded project ViewCorrect: Predictable Co-Design for distributed embedded mechatronic control systems, conducted together with the Electronic Systems group of the TU/e. His current interests are multi-disciplinary modeling, co-simulation, embedded control systems, and real-time operating systems.

Demonstrations

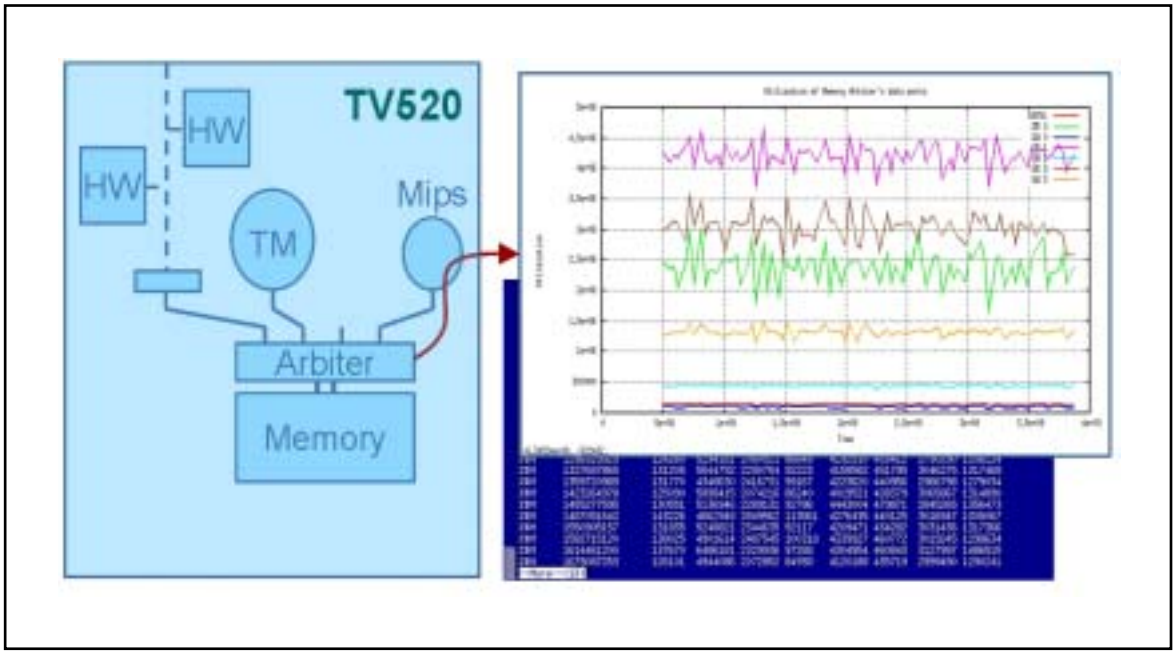
Section numbers are the booth numbers.
(see plan of Auditorium)

1 Self stabilizing TV systems

NXP Research

Overview

In many systems with different HW resources), a memory manager or arbiter regulates access towards a limited number of memory resources (e.g. shared memory). Also in the TV520, a memory manager controls the access bandwidth of each resource to the memory. Setting the access limits is a difficult task; static values may not give an optimal system performance or may even generate errors or unwanted results.
The first step towards self-stabilizing memory arbitration is gaining a precise understanding of the nature of the memory bandwidth in a variety of use cases and input video streams. The control to the memory resource ultimately is part of system-wide Quality-of-Service (QoS) management policy.



System set-up for memory bandwidth monitoring in TV520.

Method

The method on show demonstrates a near real-time monitoring of actual memory bandwidth to the three different ports of the memory arbiter inside a TV520. These ports link the memory to the control process (Mips), the Video processor (Trimedia), and various hardware IP blocks. This tool itself can help significantly in observing system behavior not only in e.g. steady state use cases, such as TV watching, but also during dynamic changes, zapping, changing to external video sources etcetera.

Benefits

Proper knowledge of the dynamics of memory bandwidth loads is crucial to find the system optimal settings or even use case adaptive settings or warnings. This helps system designers avoid overload situations and decide best possible performance/quality trade-offs. Controlled quality degradation in overload situations may minimize the user visible quality loss. Built-in hardware monitors, complemented by adaptive algorithms and Quality-of-Service policies, bear the promise of a much more robust system architecture, where the needs for worst-case design as well as exhaustive testing of all use cases is reduced. System reliability is enhanced with the safety net of a self-stabilizing TV system in place.

For more information

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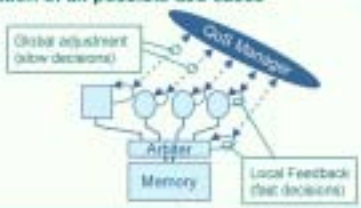
TRADER: Bus Bandwidth Monitoring "Towards Self-stabilizing TV systems"

Partner: NXP Research

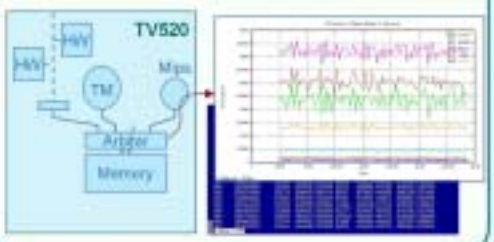
Research topic

- Adaptive, self stabilizing systems
- Traffic regulation based on actual load and use-case
- No need for worst case design and exhaustive simulation of all possible use-cases



Method on show

- First step in adaptive control: Real-time monitoring of memory utilization



Projected benefits / value

For consumers:

1. Best possible performance / quality in every configuration / operating mode
2. Overload avoidance / controlled and balanced degradation

For design & test engineers:

1. Need for worst case design reduced
2. Exhaustive use-case testing not required
3. Adapts to highest performance / quality levels possible
4. Helps in system integration and tuning of use-cases

Adoption effort needed

For Real-time monitoring:

- Limited effort: applicable with current TV sets, though limited bandwidth is available for streaming data out

For adaptive / self learning systems:

- Architect in specific monitoring functions

Place in Trader / PCP

- Runtime:
  - The adaptive system will resolve overload situations automatically in a balanced way
  - Steps in graceful degradation are distributed and coordinated, having less user perceived impact
- Design time:
  - No worst case design, hence lower cost
  - Better insight in system behavior (both static and dynamic)
  - Reduced integration and test effort

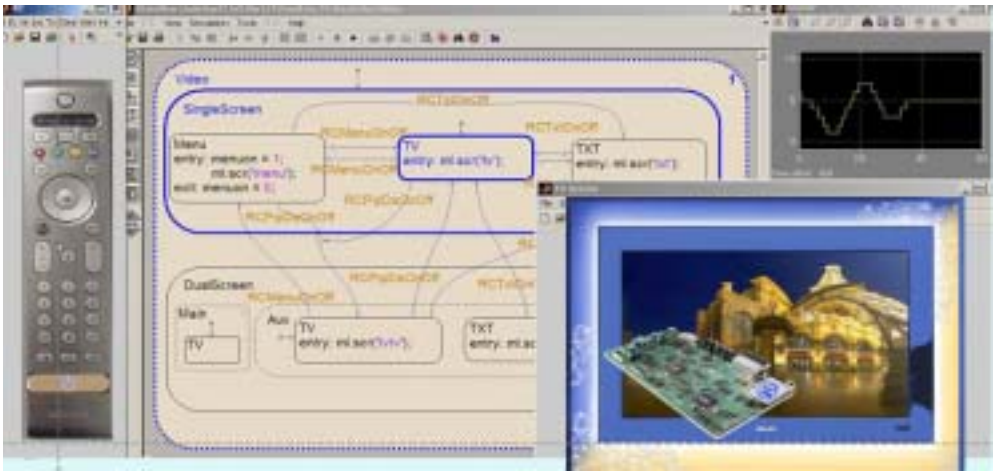
Further research planned

- Scalable & control algorithms
- Distributed control strategies for Quality of Service / Graceful degradation
- Interaction between hierarchical control loops
- Architecture support

2 Model-based awareness

Overview

Often requirements are made by writing down long lists of textual specifications. User scenarios can be written down in more or less detail, to specify what the system must do. However merely these written specifications give a limited insight in the actual behavior of a system. For a potential user it is very difficult how various features will interact (or interfere). Even architects and developers will have difficulty to grasp the full impact of these specifications.
Using a model or a set of models helps in giving early insight in the actual behavior of a system. It helps communicating with customers. Furthermore, having an *executable* model of the system behavior can also be used as a first step to give the system a form of self-awareness.



Executable requirements model of a TV

Method

The demonstration shows the power of *executable* models to allow quick feedback on the user-perceived behaviour and to increase the confidence in the fidelity of the model. In particular, executable models allow requirements engineers and customers alike to grasp the dynamic behavior of the system. The model is a first step towards model-based error detection, enabling the run-time correction of user-perceived behavior, to improve user satisfaction for a non-perfect product.

Benefits

Modeling the system helps during the requirements phase. It gives early feedback whether the system and its feature behave in line with the customer's intentions. Executable models allow early detection of requirements inconsistencies and omissions. They allow a quick customer feedback on new functionality and feature interaction. Formal model-checking techniques can improve model and ultimately system quality.
Furthermore, the model can form the basis for automated regression testing against behavorial models, codifying customer expectations.

For more information

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TRADER: Requirements Modeling
Partner: ESI

Embedded Systems INSTITUTE

Research topic

Use of executable behavioural models for requirements specification and analysis

Detect faults in requirements as early as possible.

- Missing or ambiguous requirements
- Unexpected interactions of features
- Contradicting statements, leading to inconsistent requirements

"Requirements errors are the greatest source of defects and quality problems"

"Costs of requirements error ≈
10 x costs of design error &
100 x cost of coding error"

Method on show

Creation of an executable requirements model and visualization to improve product specification

Projected benefits / value

For requirements engineers (*using simulation*):

- Early detection of incomplete, ambiguous, and inconsistent requirements
- Quick feedback on new functionality and feature interaction.

For system test engineers

- Automate testing of implementations based on behavioural model

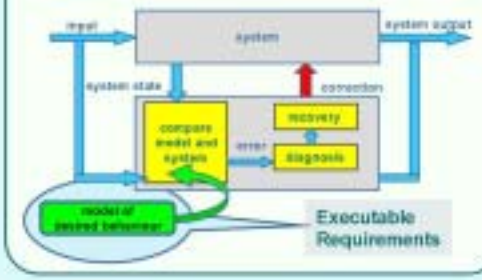
Long term vision

Model based error detection

Linux-based awareness framework for experiments with run-time error detection and correction:

Place in Trader / PCP

- Role in product design:
  - Requirements capturing and analysis
  - Testing of system and components



Further research planned

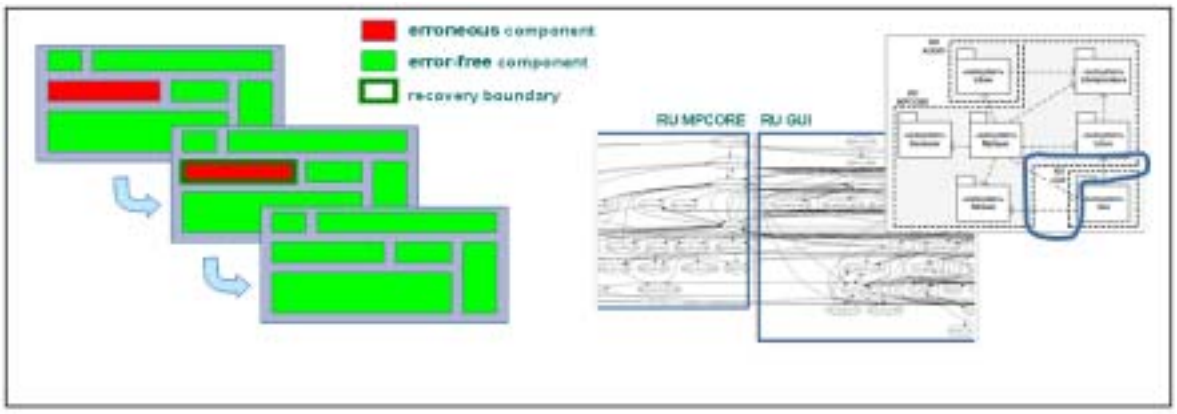
- Modeling high-level system design and investigate techniques to analyze performance and reliability aspects
- Relate requirements models to design models, check conformance
- Investigate techniques to improve model quality
- Experiment with model-based error detection
- Study feasibility of model-based testing

2a Local recovery

University of Twente

Overview

A complex application has multiple tasks running, as threads or processes on a single CPU. If an error occurs in one of the tasks, most embedded applications have to perform a full reset to start working reliably again. If however the tasks are sufficiently separated, one can consider doing local restarts of the faulty tasks.
Local recovery is more effective than global recovery for decreasing the time to recover and increasing system availability. Introducing local recovery to an existing system requires a substantial maintenance effort. Three basic requirements need to be met to introduce local recovery, which are; isolation, communication control and coordination of recovery actions.



Local recovery concept (left) and Design analysis for Recoverable Units (right)

Method

The method on show presents a framework for local recovery, and the identification of recoverable units. The framework provides a wrapper for splitting a system into a set of units. These units are isolated from each other so that they can be independently recovered. The framework further includes reusable components for communication control and coordination of recovery actions. The method is illustrated with a case study, local recovery is introduced into an open-source media player called MPLAYER. To do this, the architecture of the system must ensure that the different tasks have properly defined interfaces. Further, between the interfaces of the tasks, an extra functionality may be needed to ensure that non-faulty tasks are not influenced by tasks that run into an error.

Benefits

Local recovery is an effective approach for high availability and fast recovery. Given a good error detection which identifies which tasks have an error, it is possible to recover quickly, with only minimal effect to the user. This can prevent field calls and returns. However, the application of local recovery requires substantial development effort to support isolation and to coordinate recovery actions.

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TRADER: Local Recovery

Partner: University of Twente

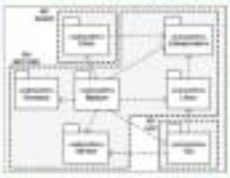
Embedded Systems INSTITUTE

Research topic

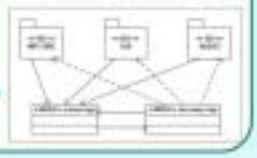
- How to design a system with local recovery?

Method on show

- FLORA: A Framework for Local Recovery
- Decomposing the Software Architecture into a set of *Recoverable Units* (RU)



•Providing isolation, communication control & recovery coordination



Projected benefits / value

For end users:
- Keeping effects of errors contained and decreasing the visibility of errors for end users

For NXP customers:
- More reliable and robust platform which reduces external visibility of errors.

For software developers:
- Way of working gives better modular design and clear interfaces

Adoption effort needed

For Software Architects:
- Selection of RUs

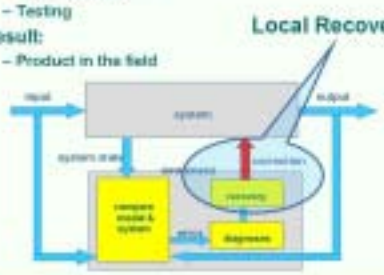
For Software Developers:
- Integrating and configuring the framework

For Testers:
- Testing recovery mechanisms by fault injection

- Can be incrementally adopted
- Fits well to the component-based design

Place in Trader / PCP

- Effort:
  - Architecture Design
  - Implementation
  - Testing
- Result:
  - Product in the field



Further research planned

- Analysis Tool Set for guiding the design decisions related to recovery
  - Optimization algorithms
  - Analytical models
- Integration with the other Trader research tracks
  - Diagnosis
  - Error Detection
- Investigation of re-engineering effort for TV
  - Re-engineering effort for MPlayer based on the Lines Of Code (LOC) written for RU wrappers:

	LOC_{RU}	$LOC_{RU\ wrapper}$	ratio
RU MPCORE	214K	463	0.22%
RU OUI	20K	345	1.72%
RU AUDIO	8K	209	2.61%
TOTAL	242K	1017	0.42%

TRADER

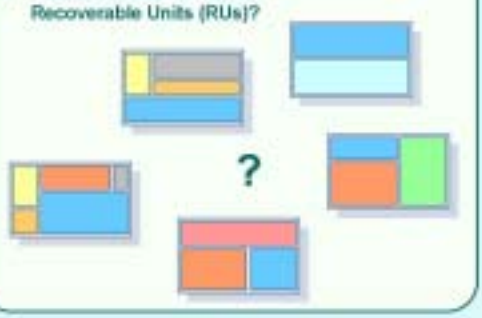
TRADER: Architecting for Recovery

Partner: University of Twente

Embedded Systems INSTITUTE

Research topic

- How to choose the set of Recoverable Units (RUs)?



Scoping the Design Space

- Based on constraints from the domain

Examples:

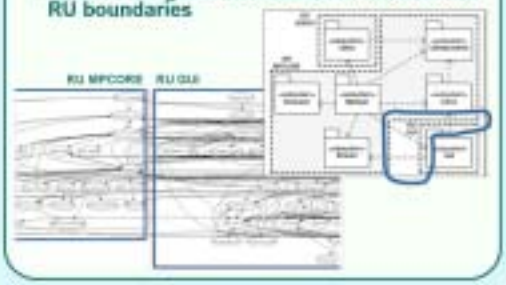
- The number of RUs must be ≤ *R*
- Modules M1 & M2 must be kept together
- Modules M5 & M7 must be placed in different RUs

Availability

- Analytical models are automatically generated for decomposition alternatives to estimate system availability based o the module properties:
  - MTTF: Mean Time To Failure
  - MTTR: Mean Time To Recover

Function Dependency

- Frequency of function calls and execution times are obtained from the *GPROF* profiler
- Queries are generated based on the selected RU boundaries

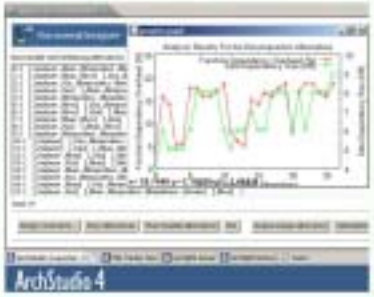


Data Dependency

- Data profiling
  - Memory accesses of modules are logged at run-time
- Profiler is implemented as an extension to the *Valgrind* tool
  - Binary code is instrumented to extract the necessary information
- Results are stored in a database
- Data dependencies between the selected RU boundaries are queried

Optimization

- *max.* availability *within*
  - Domain constraints
  - Function dependency & data dependency limits



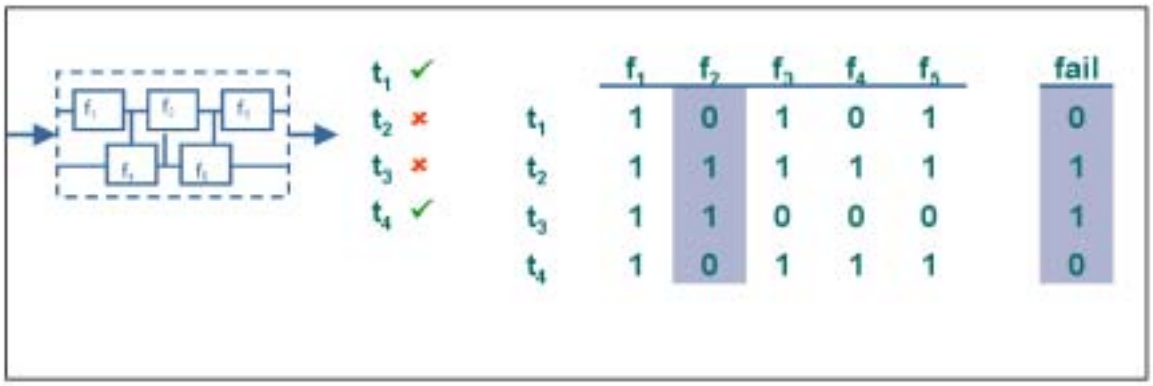
TRADER

3 Spectrum-based Fault Localization

Delft University of Technology

Overview

Some software failures are very difficult to repair. For example because they are difficult to reproduce or because it is difficult to reason about the symptoms of the error related to the architecture. These difficult problems often both take many days or even weeks to analyze and solve and require the most experienced developers or architects, which usually are very busy already.



System set-up for memory bandwidth monitoring in TV520.

As a computer-aided diagnosis technique, spectrum-based fault localization (SFL) assists in finding the root cause of failures, thus shortening the software testing and debugging cycle.

Method

SFL works by instrumenting the entire software at an arbitrary level of granularity, e.g. every function, or even every grouped set of statements, such that the execution of its various parts can be logged. As show in the figure above, we record execution traces for a number of test cases (t_1...t_4), indicating what parts of the software are involved each of them. A smart correlation between the outcome of test cases (pass/fail) and the activity of the different parts (f_1...f_5) gives a good measure of the likelihood that the different parts are involved in the failures. In order to use this method one needs an error that is at least now and again reproducible and identifiable. Furthermore, the software must also have both test cases that fail, but also and some that pass.

Benefits

Spectrum-based fault localization quickly determines the most probable locations of the root cause of observed system failures. A specific advantage of the approach is that it can be applied relatively easily, also by developers that do not have a thorough understanding of the architecture. Practical experience with SFL has indicated that in real-life development scenarios, debugging times can be reduced from weeks to days or even hours.

For more information

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TRADER: Spectrum based Fault Localization

Partner: TU Delft

Research topic

Spectrum-based Fault Localization

- Goal:
  Identify the root cause of system failures
- Approach:
  Identify the components whose behavior coincides with the occurrence of errors

Method on show

- Application in computer-aided debugging
- Control software (MIPS) instrumented to measure activity at block-level
- Evaluation on actual TV520 PRs:

Case	Inspect
NVM corrupt	96 blocks, 10 files*
Scrolling bug	5 blocks
Invisible pages	12 blocks
Tuner problem	2 files

Projected benefits / value

Developers:
- Suggestions for where to look for faults

Integrators:
- Problems found at integration testing come with an indication where they could be solved

General:
- Less dependence on experienced engineers

NXP / customer:

SFL increases the efficiency of debugging

⇒ More bugs can be fixed before release deadline

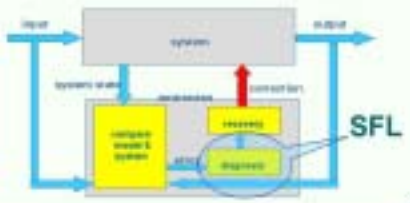
⇒ More reliable products

Adoption effort needed

- Instrumentation (2 hrs on TV520)
- Construct scenario to contrast correct and faulty behavior (typically part of PR)
- In some cases, extra test code required
- Execute tests and evaluate report
- Use output to guide error analysis

Place in Trader / PCP

- Development
- Integration
- Testing



Further research planned

Investigate relation with
- Model-based diagnosis
- Bayesian reasoning

FDIR (fault detection, isolation, and recovery) integrate with:
- generic error detection mechanisms
- recovery mechanism

For more information, see
http://nww.wiki.nxp.com/display/DTS/TraderProgramSpectra

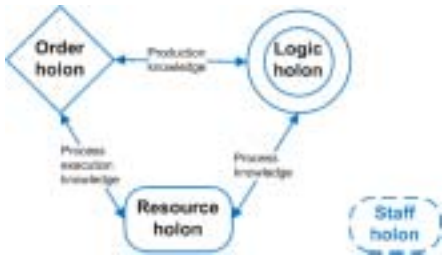
TRADER

4 Agent-based control framework

Eindhoven University of Technology

Overview

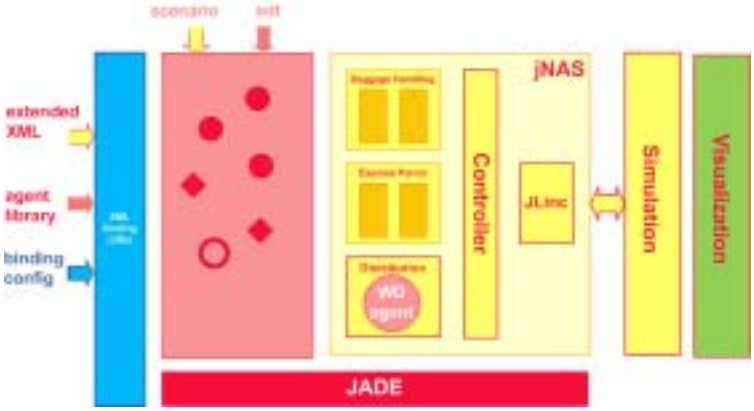
The main goal is providing a framework for the design of the high-level control of warehouses, which will enable quick experiments with different control strategies. We aim to achieve a hierarchical control structure, which separates the system concerns and pushes decision making as low in the hierarchy and as late as possible, making the system more flexible and more adaptable to changes.



To achieve these goals, we chose to use the holon concept as the basis of the high-level control design, because it provides a clear separation of the resources in the system (resource holons), the tasks to be performed (order holons), and task execution (logic holons) [1]. For the implementation of the holons, we selected JADE agent middleware, which provides a standard design approach, protocols for agent communication, and support for distribution of agents over different hosts [2].

Method

We tried to integrate the framework within Vanderlande Industries' way of working by using the Sandglass model and the new architecture for simulation (NAS). The input of NAS includes a project definition file, which represents a warehouse layout (an XML file based on the Sandglass model). This layout is used to generate a hierarchy of resource and logic holons: each component in the layout is represented by a resource holon and a logic holon, which is responsible for registering the services provided by resource holons corresponding to its children.



To allow experiments with different holon behaviors, the NAS project definition file is extended with agent metadata, which specifies which behaviors to select from a pre-developed agent library. Order holons are created from the initialization information of NAS: customer orders are generated from the scenario input, which represents orders to be fulfilled. The interaction of the different generated holons allows orders to be fulfilled. This order fulfillment can be visualized using NAS' interface to simulation tools like Automod.

Benefits

The holonic approach allows easy design of components of very complex systems: a system is represented by a large number of simple components, which can be designed (relatively) independently from each other. The hierarchical structure provides scalability (by restricted holon interaction) and fault tolerance (by local exception handling).

The framework is based on Vanderlande Industries' tooling (NAS) and mature agent middleware (JADE), which increases the usability and maintainability of the framework.

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[2] Fabio Bellifemine, Giovanni Caire, Agostino Poggi, and Giovanni Rimassa, JADE: A software framework for developing multi-agent applications. Lessons learned, Information and Software Technology 50(1-2): 10-21, January 2008.

For more information

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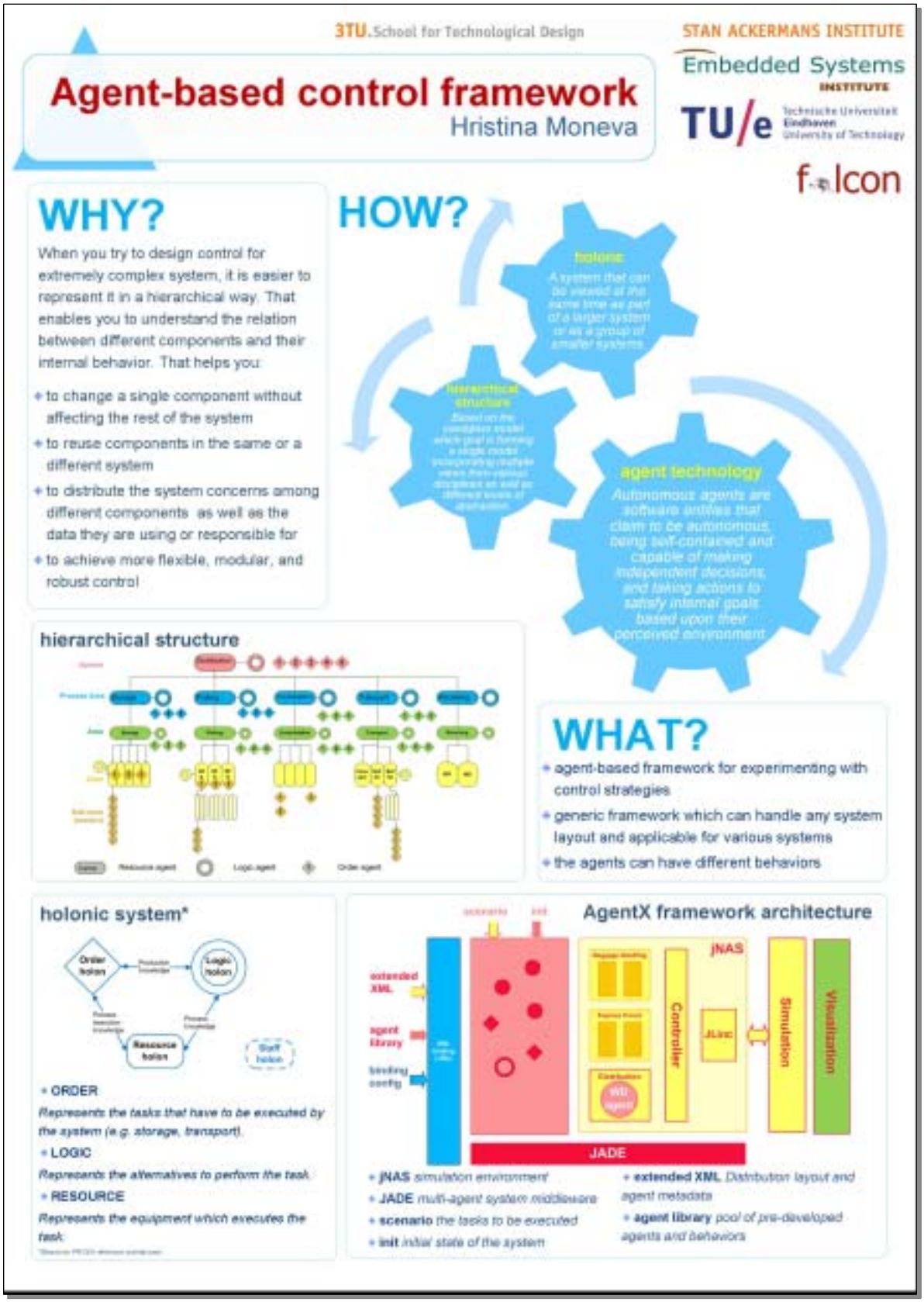

3TU. School for Technological Design
STAN ACKERMANS INSTITUTE
Embedded Systems INSTITUTE
TU/e Technische Universiteit Eindhoven University of Technology
f.falcon
Agent-based control framework
Hristina Moneva
WHY?
When you try to design control for extremely complex system, it is easier to represent it in a hierarchical way. That enables you to understand the relation between different components and their internal behavior. That helps you:
to change a single component without affecting the rest of the system
to reuse components in the same or a different system
to distribute the system concerns among different components as well as the data they are using or responsible for
to achieve more flexible, modular, and robust control
HOW?
holonic
A system that can be viewed at the same time as part of a larger system or as a group of smaller systems
hierarchical structure
agent technology
Autonomous agents are software entities that claim to be autonomous, being self-contained and capable of making independent decisions, and taking actions to satisfy internal goals based upon their perceived environment
hierarchical structure
WHAT?
agent-based framework for experimenting with control strategies
generic framework which can handle any system layout and applicable for various systems
the agents can have different behaviors
holonic system*
Order holon
Logic holon
Resource holon
Staff holon
ORDER
Represents the tasks that have to be executed by the system (e.g. storage, transport).
LOGIC
Represents the alternatives to perform the task.
RESOURCE
Represents the equipment which executes the task.
AgentX framework architecture
extended XML
agent library
binding config
jNAS
Controller
JLisc
Simulation
Visualization
JADE
jNAS simulation environment
JADE multi-agent system middleware
scenario the tasks to be executed
init initial state of the system
extended XML Distribution layout and agent metadata
agent library pool of pre-developed agents and behaviors

5 Order picking by underactuated robot hands

Delft University of Technology – BioMechanical Engineering

Background

For fully automated order picking, the handling of irregularly shaped items is challenging. Conventional solutions like vacuum technology are not suited because of the irregular shape of the items. Dedicated, fully actuated solutions are too expensive because of the typically large number of different items in a warehouse.
In this research, we design robot hands that intrinsically adapt to the shape of the items. To obtain this *shape adaptation* without a complex control architecture, we make use of *compliant, underactuated mechanisms*. Underactuated means that the number of actuators of the hand is less than the number of moving joints; while compliant means that the hands consists of elastic elements that passively deforms under a load (see Figure 1 for an example of an compliant, underactuated finger mechanism).

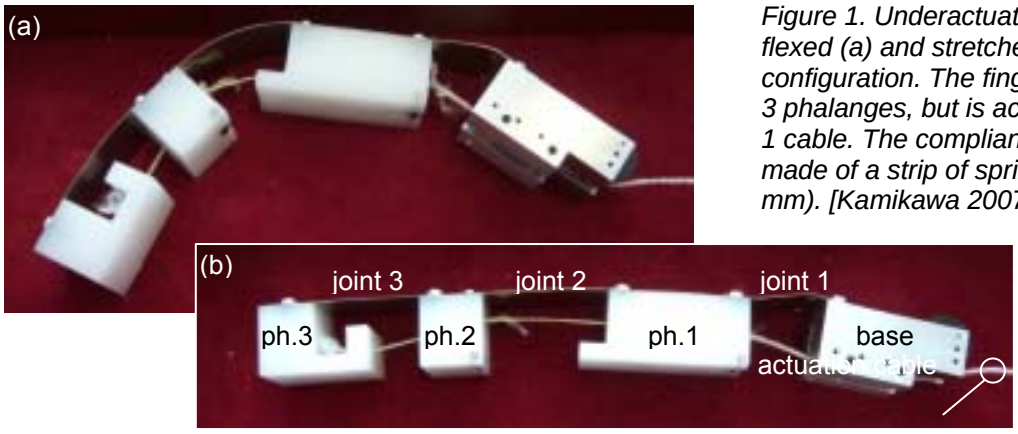
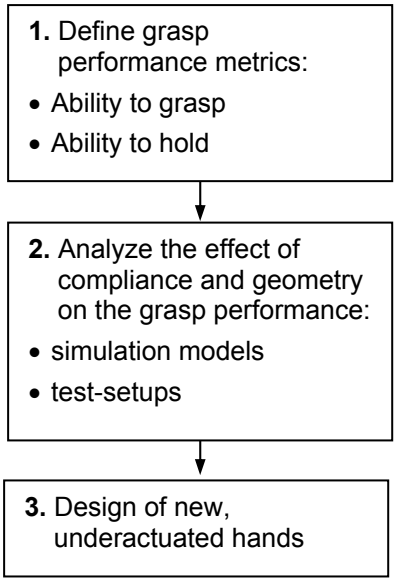


Figure 1. Underactuated finger in flexed (a) and stretched (b) configuration. The finger consists of 3 phalanges, but is actuated by only 1 cable. The compliant joints are made of a strip of spring steel (0.1 mm). [Kamikawa 2007, TUD]

Method

To design compliant, underactuated robot hands, firstly a grasp performance metric must be defined. For this metric, we distinguish the ability *to grasp* and *to hold* an item. Grasping means that the hand is able to obtain equilibrium with items of different size on different locations. Holding means that a grasp is maintained, even when subject to disturbances like for instance acceleration and deceleration.
Secondly, we analyze the effect of compliance and geometric parameters of the hand on the grasp performance. Based on this analysis in simulation models and test-setups, we determine the parameters that mainly influence the performance.
Thirdly, we define design rules and apply these on the design of two prototypes. One prototype will be optimized with respect to the ability to grasp and hold a large number of different items. The second prototype will be optimized with respect to minimizing the number of parts (and hence costs), while still be able to grasp and hold an item.



Relevance

The benefits of underactuated robot hands compared to fully actuated hands are the reduction of actuators, sensors and control complexity without necessarily reducing the grasp performance. Hence a reduction in costs and an increase in robustness can be expected from this approach.

For more information

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Order picking by underactuated robot hands

Irregular objects grasped by simple mechanisms

Design Problem

- Unknown relation between Design Choices and Grasp Performance.
- No suitable Grasp Performance metric exists for Compliant, Underactuated hands.

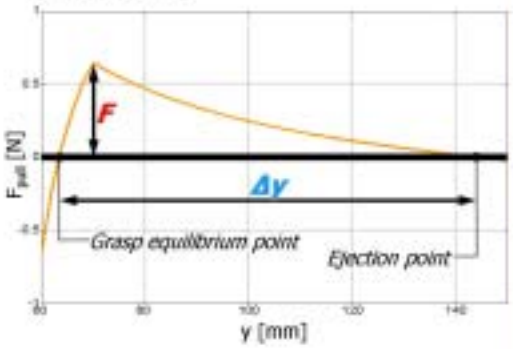
Grasp Performance

1. Ability to grasp
Quantify: Basin of attraction (*Δy*) resulting in a stable grasp.

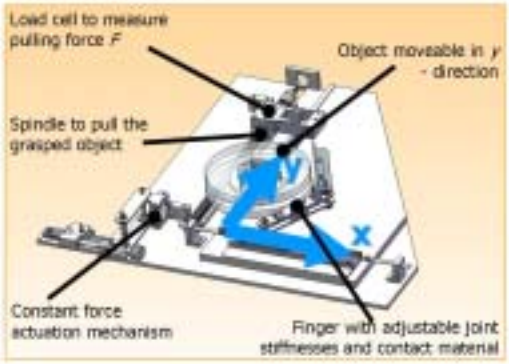
2. Ability to hold
Quantify: Minimal force (*F*) needed to pull the object out of the hand.

Approach

Simulations:



Measurements:



Acknowledgement
This work has been carried out as part of the FALCON project under the responsibility of the Embedded Systems Institute. This project is partially supported by the Netherlands Ministry of Economic Affairs under the Embedded Systems Institute (BSIK03021) program.

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Embedded Systems INSTITUTE f-Icon TU Delft

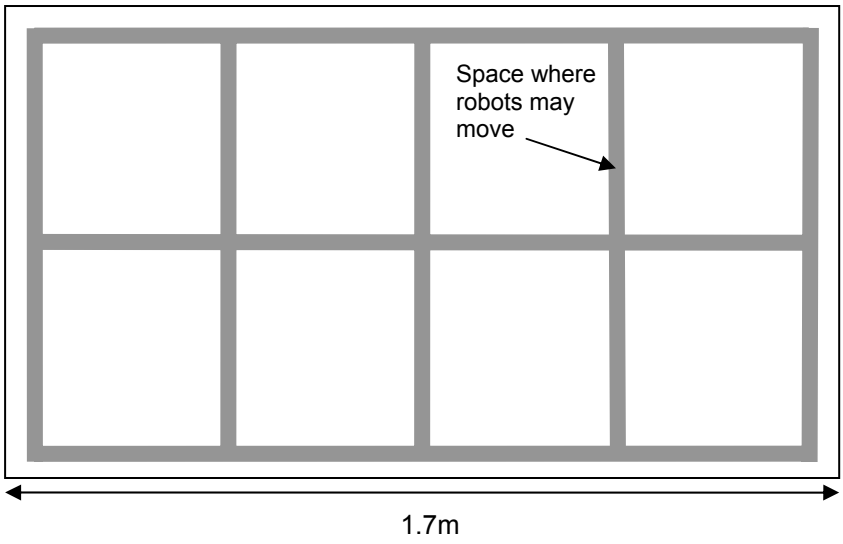
Delft University of Technology

6 Coordination of autonomous shuttles

Overview

Currently warehouse transportation systems are generally built using conveyors. Usually the number of conveyors is kept to a minimum to cut down on costs. This means that when one section of a transportation system breaks down, a large part of the system will become unavailable. This problem can be overcome by including redundant conveyors, but this is a very expensive solution.
Autonomous shuttles that move around freely do not have this vulnerability of the traditional conveyor systems. If a shuttle breaks down and obstructs a part of the transportation system, the other shuttles can dynamically alter their paths to move around it.
If many shuttles are moving around at the same time, their operations should be coordinated in such a way that they do not collide and deliver goods on the correct time at the correct place.
Scenario
To research different coordination methods, we start on a small scale with a set of small robots (e-pucks) shown in the figure below. We let a number of e-pucks perform transportation tasks in a simple warehouse layout. Five e-pucks are available that will move around within an area of 1.3m x 1.7m. A camera on top keeps track of their positions.
For every e-puck we have implemented an application that receives the position of an e-puck, and controls the e-puck along predefined paths. Below, an example layout is shown. The e-puck applications ensure collision-free robot motions.
In a real warehouse many shuttles may be active. We can simulate this by adding virtual e-pucks to the running system. The controllers of the e-pucks cannot distinguish between virtual and a real e-pucks. In our demonstration we will show a virtual 3D representation of the predefined layout of the robot paths and all e-pucks (real and virtual) moving along these paths.

E-puck robot



Example layout of robot paths within the demonstration area

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Coordination of autonomous shuttle

TU/e Technische Universiteit Eindhoven University of Technology

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Dynamics and Control
Mechanical Engineering

falcon
Flexible Automated Logistics CONcepts

Problem Definition

→Flexible and robust control of the transportation in distribution centre

→More decisions made by the low level control, i.e: autonomy

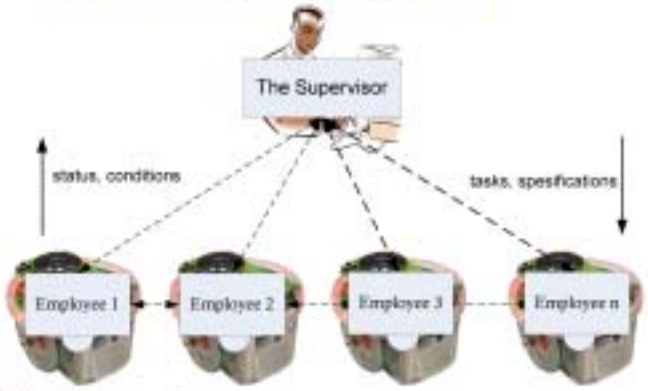
How?

Autonomous Shuttle

→Shuttle that autonomously determines its trajectory and movement when given a task

→A number of shuttles are coordinated to accomplish set of tasks

Control and Responsibility



The Supervisor

→ Giving tasks, reference path, global collision avoidance

The Employee

→ Tracking control, optimizing speed, local collision avoidance

Experimental Setup

Requirements

→ Accurate trajectory tracking
→ Shuttles must not collide
→ Overtaken is not allowed

Supervisor …

1. selects desired employees
2. assigns them tasks

Research challenge

Optimal and *robust* task execution

- *Optimal* → time, energy, resources …
- *robust* → obstacle avoidance, collisions-free, no deadlocks & livelocks, …

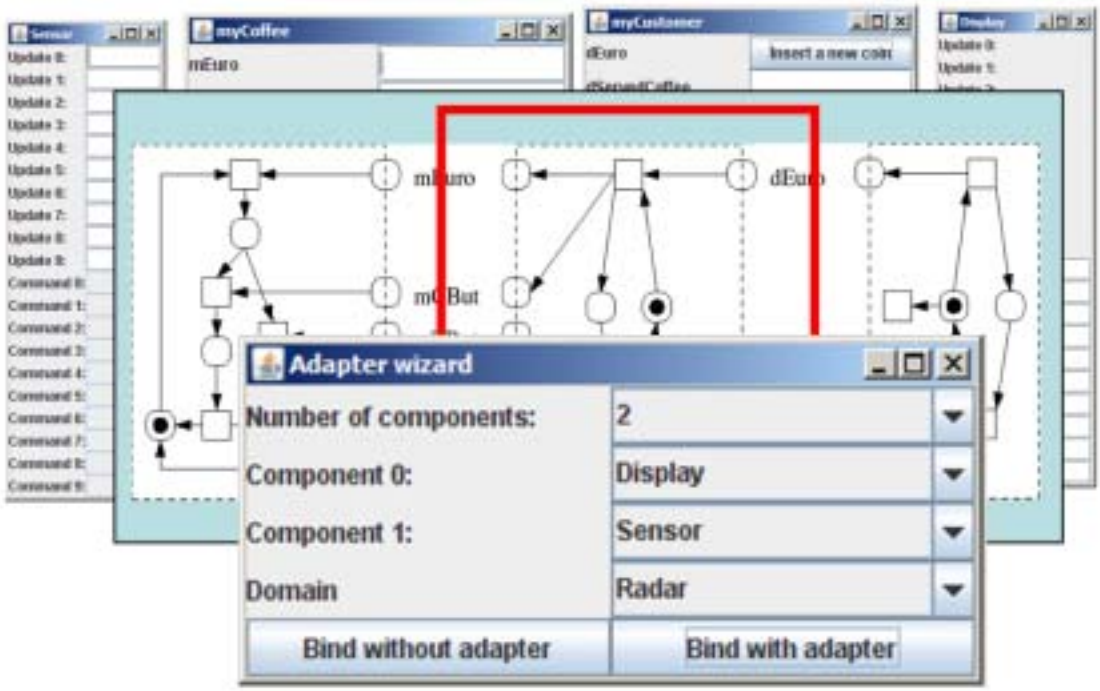
This work has been carried out as part of the FALCON project under the responsibility of the Embedded Systems Institute with Vanderlande Industries as the industrial partner. This project is partially supported by the Netherlands Ministry of Economic Affairs under the Embedded Systems Institute (BSIK03021) program.

7 Semi-automatic adapter (glue logic) generation

TU Eindhoven - Architecture of Information Systems Group

Overview

A challenge in the development of systems-of-systems (SoS) is the fast and run-time integration of existing systems. In many cases, these systems have been developed independently, and no domain-specific standard for interoperability exists. In such cases a dedicated adapter is needed. Adapters can be constructed on the basis of models (e.g., simulators) of the interface behaviour of the systems. We study the (semi-)automatic generation of behavioural adapters on the basis of models of the given systems.



Method

In this demonstration we show adapter generation using the research tool Fiona. Each system is described by a behavioural interface model, which may be derived from, e.g., protocol standards, partial (data) models, technical agreements, and event logs. In addition, the adapter specification consists of a behavioural property (e.g., deadlock-freedom) and a set of elementary data transformations. Adapters are computed using a controller generation algorithm that is based on state-space exploration. By construction, the generated adapters establish the behavioural property while only using the given data transformations.

Benefits

The approach distinguishes between two different aspects: the interaction protocols, and the data conversion. Reuse is facilitated for both aspects. The interfaces models of the given systems are reusable for integration with other systems. Furthermore, existing data conversion routines can easily be reused.

The approach generates adapters with highly-parallel interaction protocols, which establish certain properties by construction. The approach moves the focus of the integrator and the tester from the adapter to the existing systems and the domain knowledge; thus reducing the required effort and time for building adapters.

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Poseidon: Adapter generation

TU/e - Architecture of Information Systems Group

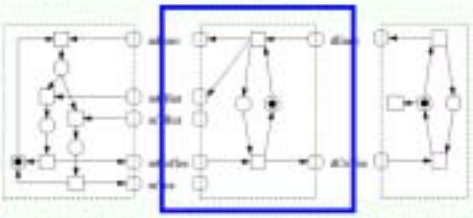
Embedded Systems INSTITUTE

Research topic

Semi-automatic adapter (glue logic) generation:

"behavioural adapters based on requirements and models of the interface processes"

- Application area: fast integration of MSS SoS



Method on show

Adapter generation using the tool Fiona:

- Based on state-space exploration
- Most-permissive adapters: featuring all behavior

Projected benefits / value

For System Integrators:

"generate behaviour/protocol of adapters"

- Based on reusable models of existing systems
- Separate data conversion from protocol
- Reuse of existing code for data conversion
- Generation of highly-parallel protocols
- Less development time and effort

For Testers:

"some requirements hold by construction"

- Validation of models can be done before testing
- Testing can focus on higher-level requirements

Adoption effort needed

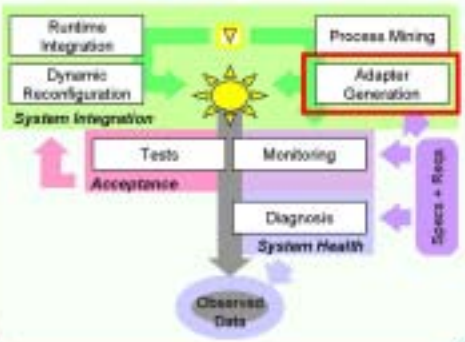
For System Integrators :

- Develop good interface models
- Make requirements on adapters explicit
- Integrate existing low-level interfaces
- Formalize domain knowledge

For Testers :

- Validate the interface models before integration
- Formalize low-level requirements on adapters

Place in Poseidon



Further research planned

How to obtain interface models:

- Process mining from execution logs
- Extract from available data models

Requirements on adapters:

- Behavioural properties like deadlock-freedom
- Data transformations that can be applied
- Behavioural completeness of the adapter

Automatic adapter generation:

- Other approaches to generate adapters
- Parameterization and composition
- Dealing with incomplete models

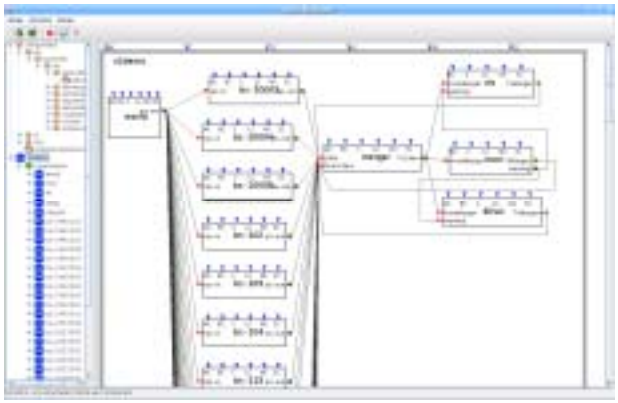
TU/e

8 Runtime integration

TU Delft – Embedded Software Laboratory

Overview

Maritime Safety and Security Systems-of-Systems (MSS SoS) require abilities for extension and reconfiguration at runtime. The objective here is to allow for the join-and-leave of systems (such as AIS base stations) with the SoS running and fully operational. Additionally, it should be possible to add new functionalities or to update a part of the system with minimal efforts and without interfering the SoS' operations.



Representation of the SoS as components.

Display of the data merged and monitored.

Method

The current approach uses a component-based representation of the system. Each component is independent from the others, has explicit inputs and outputs, and has a special set of interfaces to allow runtime management (e.g.: start/stop, add sub-components…). The current implementation is done in the ATLAS platform.

The second part of this demonstration is the integration and monitoring of the system. The created system is representative of an MSS system. AIS base stations receive data from the boats (instantiated via a 'world' component). The data is merged by a dedicated component, which offers a global picture that can be accessed via a specific protocol. This picture is used by various visualization components. Additionally, a special AIS data monitoring component is connected to the 'merger'-component in order to detect data which is either non-conformant to the standard or inconsistent.

Benefits

System integrators benefit the most of this work, as it permits them to update components at runtime, and integrate (or remove) systems as they become available (or leave). Further, it enforces the definition of each part of the system as a component, which promotes reliability and software evolution. The monitoring capabilities should ease the work of test engineers and help the operators to associate confidence with displayed data.

However, the primary goal of this work is to lay the foundation for further research. In particular, we will focus on automatically deriving the components and monitors from UML specification of the SoS. Moreover, we will study how to integrate systems based on different architectures (client/server, publish/subscribe…). We plan to explore the possibility of associating geographical data to components so that the SoS layout can be represented next to the observed information.

For more information

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Poseidon: MSS Runtime Integration

TU Delft – Embedded Software Laboratory

Embedded Systems INSTITUTE

Research topic

Runtime Integration of Components:
Reconfiguration of the system without stopping it

Method on show

Track Merging:
- Multiple AIS base stations
- One global picture
- New components can have direct knowledge of the latest picture.

Join and Leave:
- Component-based system
- Components can be aware of life-cycle and of bindings

Monitoring of AIS Data:
- Reports the protocol errors on the display

Based on the ATLAS platform.

Projected benefits / value

For Component Engineers:
- Clear definition of the components

For System Integrators:
- Can update a component at runtime
- The MSS can be extended easily, at any time, with new functionality.

For Test Engineers:
- Simplifies the monitoring infrastructure

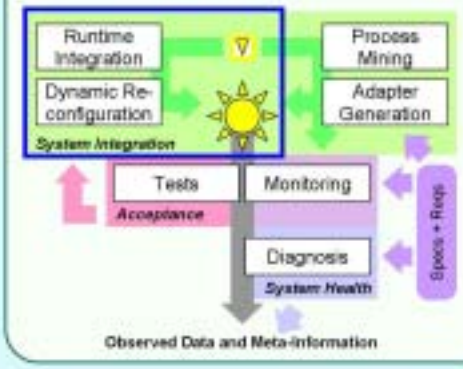
For Operators:
- Can link level of QoS to components

Adoption effort needed

For Component Engineers :
- Need to handle explicitly modifications of the bindings (but could be automated by the platform, e.g. not needed in DDS)
- Express the components properties (input, output...) in an Architecture Description Language (ADL)

For Test Engineers:
- Adapt tools to the new infrastructure

Place in Poseidon



Further research planned

- Add a geographical view of the system to relate errors to the position of the components
- Derive the component interface signature from the specification model (e.g.: in UML)
- Derive the monitors from the protocol specification
- Integrate with adapter generation
- Generalize and extend the approach to support mixed architectures (C/S, Pub/Sub...)
- Infrastructure to associate attributes (e.g. QoS level) to data streams

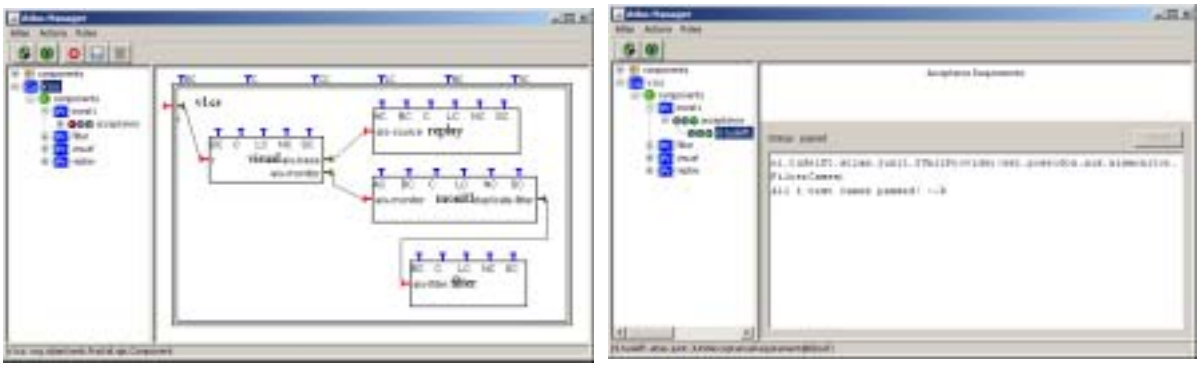
TU Delft

8a Runtime acceptance

TU Delft – Embedded Software Laboratory

Overview

Maritime Safety and Security Systems-of-Systems (MSS SoS) have a dynamic nature, and depend on high availability of services they provide. Sub-systems join and leave during operation, and these runtime modifications and reconfigurations pose threats to the stability of the overall MSS SoS. Before applying a runtime reconfiguration, it must be guaranteed that the change will not break anything. Ideally, verification of the applied changes and their acceptance should be fully automated.
Within the Poseidon project, TU Delft is working to provide techniques and tools that support runtime evolution through dynamic verification and acceptance.



MSS system-of-system with added testing and acceptance information

Method

Automation of the runtime testing and acceptance process requires the underlying runtime platform to support Acceptance Interfaces and Testing Interfaces, two extensions of the built-in test paradigm developed within Poseidon. The first provides a way of associating integration tests of components with the components themselves, and notifying each other of changes in their environment. That way, components are made responsible for verifying their own dependencies automatically. The latter provides means for testers and system integrators to control and better observe the tested components.
The current implementation of the techniques is based on JUnit (junit.org) and the Fractal component model (fractal. openweb.org). It can be transferred to the testing tool chain of Thales, the carrying industrial partner of the project, and also to OpenSplice or other publish-subscribe architectures used within such industries.

Benefits

Acceptance and Testing Interfaces will allow the automated verification of the system during development, or when part of the system changes during runtime. This automation is directed towards reducing the cost, in time and resources, of the system verification at system integration and acceptance levels. Quality-of-Service or conformance information produced by the tests is stored with the components and thus becomes available to enhance the situation-awareness view with system-awareness information.

For more information

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Poseidon: Runtime Acceptance

TU Delft – Embedded Software Laboratory

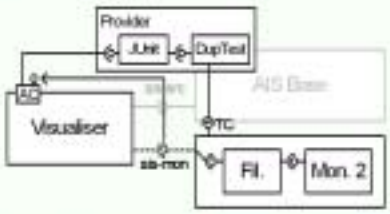
Embedded Systems INSTITUTE

Research topic

Runtime Acceptance of Components:
Assuring that component's expectations are met.

Method on show

Atlas Built-in Acceptance Testing:



Components are responsible for checking their new environment, and v.v., before (re-) starting

Projected benefits / value

For Integration Engineers:
- Simplified testing
- Architectural changes are verified by the components before performing a change.

For Test Engineers:
- Tests are associated with the components, but still separated from the component functionality.
- Test requests are issued by the components when needed.

For Component Engineers:
- Separation of component and acceptance functionalities

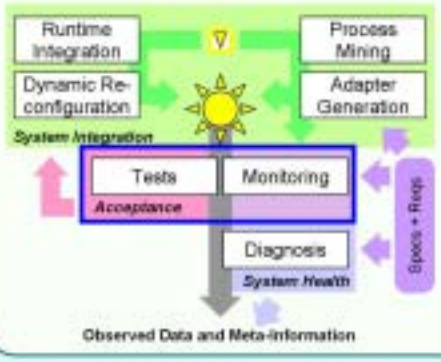
Adoption effort needed

For Integration Engineers:
- Definition of acceptance policies

For Test Engineers:
- Some test cases have to be adapted to be run in the built-in environment way.
- Test tools and providers have to be developed for the MSS platform.

For Component Engineers:
- Must specify explicitly their expectations

Place in Poseidon



Further research planned

Transfer to the Publish-Subscribe World:
- Implementation of Atlas for OpenSplice
- Tackle specific issues of testing pub-sub

Improvement of the Framework:
- Easier definition of test cases: *impersonators*
- Optimization of runtime test support

Generation of test cases:
- Model-based testing (e.g. from UML models)

Runtime Testing:
- Unwanted interaction of test & normal behavior
- Test-sensitivity
- Test-awareness

TU Delft

9 Autofocus algorithms in electron microscopy

Eindhoven Technical University – Mathematics and Computer Science

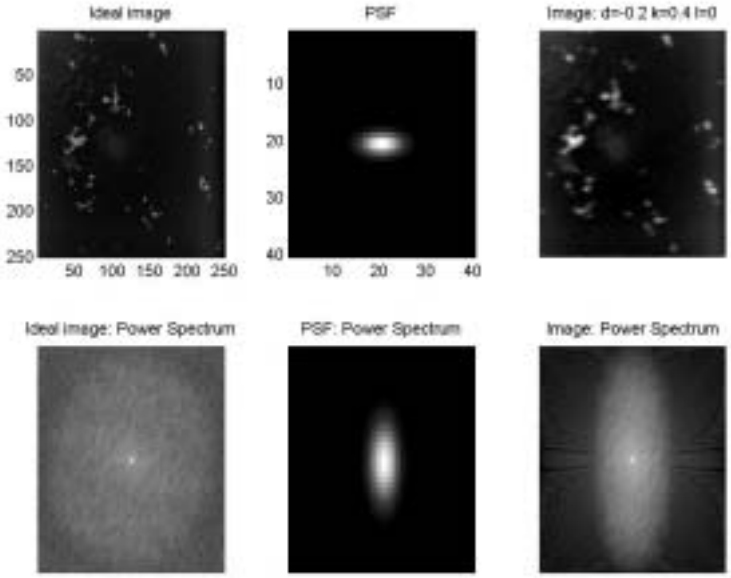
Overview

The resolving power of the light microscope (the smallest distance between two discernible dots) is 200 nm. It is limited by the wavelength of the visible light. The wavelength of electrons is much smaller (for 100-keV electrons, it is 3.7 pm). In the Scanning Transmission Electron Microscope (STEM) an electron probe is scanned over the specimen and the transmitted electrons are collected to form an image.

FEI's Titan STEM.

The ultimate goal of the research is to automate the electron microscope's controls for inserted specific specimen, in order to get images, that are in-focuse, astigmatism free, etcetera, without the aid of the user. The STEM's Signal-to-Noise-Ratio (SNR) is worse than in light microscopy due to the limited electron dose that can be applied to the specimen. Automation is complicated by the fact that only the images can be used as a source of information.

Methods



For modelling the image formation process the approximations of the Gaussians and the Fourier analysis are used.

For the image analysis the research currently focuses on Fourier, Wavelet, gradient and autocorrelation-like techniques to estimate and calculate the amount of defocus and astigmatism. The suitability of such existing techniques for the particular images is determined.

Benefits

The Condor project is turning electron microscopes from imaging into measuring instruments. It is planned to turn the electron microscope from a human-dependent device into a man-independent tool.
The research results will help to automate a Scanning Transmission Electron Microscope; autofocus and automated astigmatism correction algorithms will be developed.

For more information

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Autofocus algorithms in electron microscopy

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The Electron Microscope

The resolving power of the light microscope (the smallest distance between two discernible dots) is 200 nm, it is limited by the wavelength of visible light. The wavelength of electrons is much smaller:

$$\lambda = \frac{h}{\sqrt{2meE}},$$

where h is Planck's constant, E is the accelerating voltage, e and m are the electron's charge and mass. For 100-keV electrons, $\lambda = 3.7$ pm. In Scanning Transmission Electron Microscope (STEM) an electron probe is scanned over the specimen and the transmitted electrons are collected to form an image.

FEI's Titan STEM.

Objective

The goal of this project is to automate the focus process in STEM, which is traditionally performed by a human operator. The STEM's Signal-to-Noise-Ratio (SNR) is worse than in light microscopy due to the limited electron dose that can be applied to the specimen. Only the images can be considered as an information source, that complicates the automation.

Defocus modeling

The shape of the scanning beam in STEM is close to a Gaussian distribution. Thus, a defocused image f can be modeled as

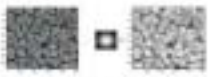


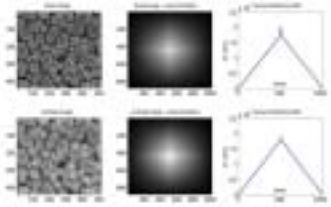
Image convolution with Gaussian.

$$f = f_0(x) \circ g(x) =: \int_{-\infty}^{+\infty} f(x')g(x' - x)dx',$$

where f_0 is in-focused image, $\circ$ is the convolution operation and $g(x) = e^{-(\frac{x}{2\sigma})^2}$.

Autofocus Methods

- Gradient and variance-based sharpness measurements: $s = \|f - c\|$, c - constant.
- Estimate image Auto-Correlation (ACR) peak.

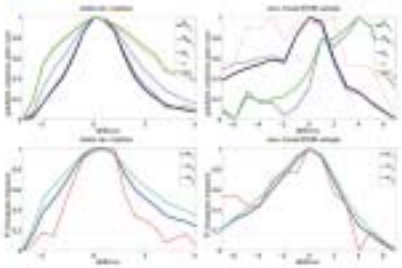


- Defocus information can be derived from the Fourier Transform (FT) of an image

Gold-on-Carbon in-focused and defocused images, absolute values of their FT

$$\mathfrak{F}[f(x)] = \mathfrak{F}[f_0(x) \circ g(x)] = \mathfrak{F}[f_0(x)]\mathfrak{F}[g(x)].$$

Experiments



Gradient, variance and ACR sharpness measures were calculated for Gold-on-Carbon and non-trivial STEM sample focus series. For the second one simple methods fail: More than one maximum appears. FT sharpness measures worked for both samples.

Acknowledgments

This work has been carried out as a part of the Condor project at FEI company under the responsibilities of the Embedded Systems Institute (ESI). This project is partially supported by the Dutch Ministry of Economic Affairs under the BSIK program.

10 Printer datapath analysis

Objective

To quantify the performance of the digital datapath of professional printing systems, considering performance measures such as throughput, page and print job latencies, memory usage, and utilization of datapath components, aiming at early datapath-architecture design-space exploration.

Partners

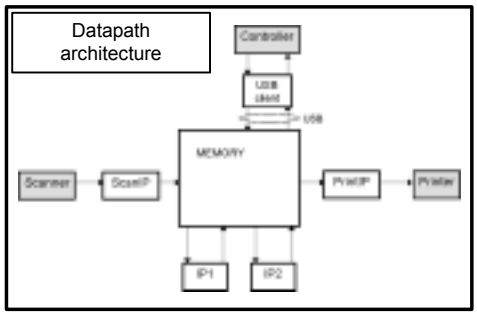
Eindhoven University of Technology (TU/e)
Embedded Systems Institute (ESI)
Océ Technologies
Radboud University Nijmegen (RUN)

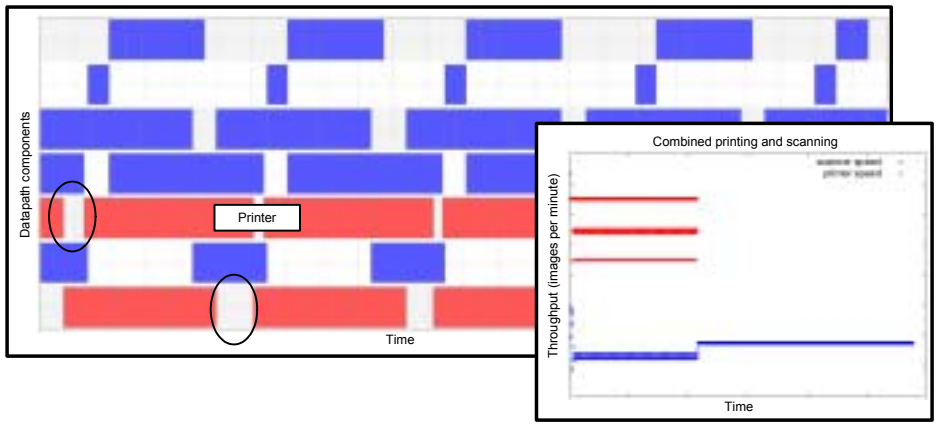
Applied Techniques

Dataflow analysis, supported by the SDF3 toolkit, www.es.ele.tue.nl/sdf3.
Timed-automata model checking, supported by the tool Uppaal, www.uppaal.com.
Coloured Petri Nets, supported by the tool CPN Tools, wiki.daimi.au.dk/cpntools/.

Results and Benefits

The analyses allow to quantify and visualize performance measures, to identify bottleneck- and underutilized datapath components, and to study transient and steady-state behavior and interference between jobs running in parallel. These results can be used for datapath design-space exploration, investigating for example alternative memory architectures, memory allocation and arbitration strategies, scheduling policies, and the impact of the speed of processing components.





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Printer Datapath Analysis

Octopus project

Embedded Systems INSTITUTE

Professional printing systems

Objective

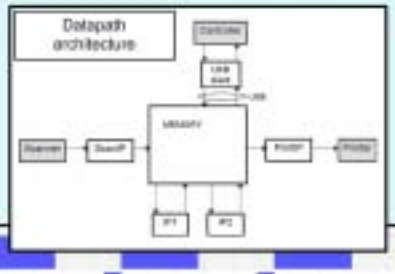
Early design-space exploration of printer-datapath architectures:

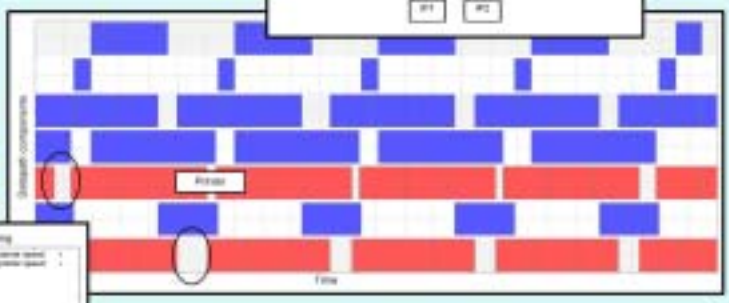
Quantify performance:

- Throughput (images per minute)
- Latencies, among others,
  - Page latency
  - Job latency
- Memory usage
- Bandwith usage
- Datapath component utilization
- etc.

Benefits and results

- Quantification and visualization of performance measures
- Identification of bottlenecks and underutilized components
- Insight in
  - transient and steady-state behavior
  - interference between parallel jobs
- Design-space exploration:
  - memory architectures
  - memory allocation and arbitration techniques
  - scheduling policies
  - alternative datapath components
  - etc.





Applied techniques

- Dataflow analysis:
  sdf3 toolkit, www.es.ele.tue.nl/sdf3
- Timed-automata model checking:
  Uppaal, www.uppaal.com
- Coloured Petri Nets:
  CPN Tools, wiki.daimi.au.dk/cpntools/

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Yang Yang (TU/e, y.yang@tue.nl)

http://www.esi.nl/octopus

Embedded Systems INSTITUTE océ TU/e

11 Probabilistic graphical models for adaptive control

Radboud University Nijmegen

General idea

The behavior of system components and their relationships can be expressed using graphical probabilistic models that succinctly represent joint probability distributions. With relatively simple and understandable models it becomes possible to reason about component observations, actions and their relations.

Case: Adaptive control for printers

This technique was applied to a printing process. In a probabilistic model, the available power for heating the paper, the temporal properties of heating components, different paper weights, minimum temperature requirements for high quality prints, and the basic process speed, have been related.
Subsequently, this model can be applied to construct a controller that regulates set points (e.g. of a heater component) on the basis of some observables (e.g. temperatures) and other properties which are unknown (e.g. paper glossiness) but probabilistically related. This simple approach has lead to controllers with some surprising characteristics and features.
As an example, a controller target can be either stated as `keep the temperature as close as possible to a certain value' or as `regulate the temperature such that its probability to decrease to a certain value is less than x%'. The second option leads to a kind of smart buffer behavior: for light paper, the temperature is regulated at a higher set point in order to account for the possibility that heavier paper will arrive.
Such behavior can be built into a rule-based controller as well, after the designer has become aware of this fact. In the probabilistic model-based controller this behavior follows automatically from the system knowledge that is captured in the model itself.

Relation to classifiers

Another example of the usefulness of these types of models is the possibility to construct diverse classifiers. Building completely black-box type classifiers, when an exact physical model is not achievable, is not favorable, as these are quite inflexible.
The probabilistic models that reflect system relationships at a global level could be interpreted as grey box models that enable a system engineer to deduce multiple classifiers. Used in such a way, this approach is more amenable to evolving system designs.
A research challenge is to build adaptive controllers on basis of probabilistic models that allow sensible trade-offs at run-time in order to achieve the required system performance.

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Control of Printer Adaptability using Bayesian Networks

Arjen Hommersom[1], Peter Lucas[1], René Waarsing[2], Pieter Koopman[1], Roelof Hamberg[3]

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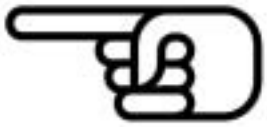
océ

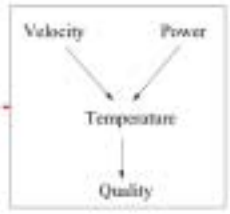
Tired of making impossible controllers for adaptable products?



Problem

- Context: adaptability
  - dynamic in-product trade-offs
  - between various qualities of operation
  - at system level
- Explicit modeling of physical processes ⇒ complex, not always feasible
- Sensor data requires interpretation ⇒ handle resulting uncertainties

Bayesian network approach

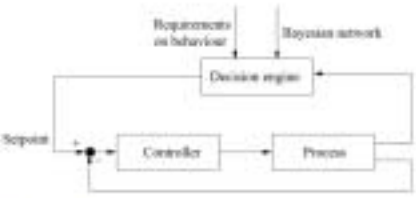


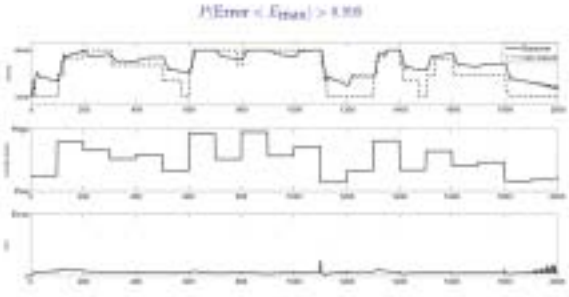
Understandable!

Structured!

Versatile!

Dynamic print speed adjustment





Discussion

- Productivity improved compared to rule-based system
- Logic of controller for free
- Required for this controller:
  - qualitative model
  - data
  - (probabilistic) requirements on behaviour

Future challenges

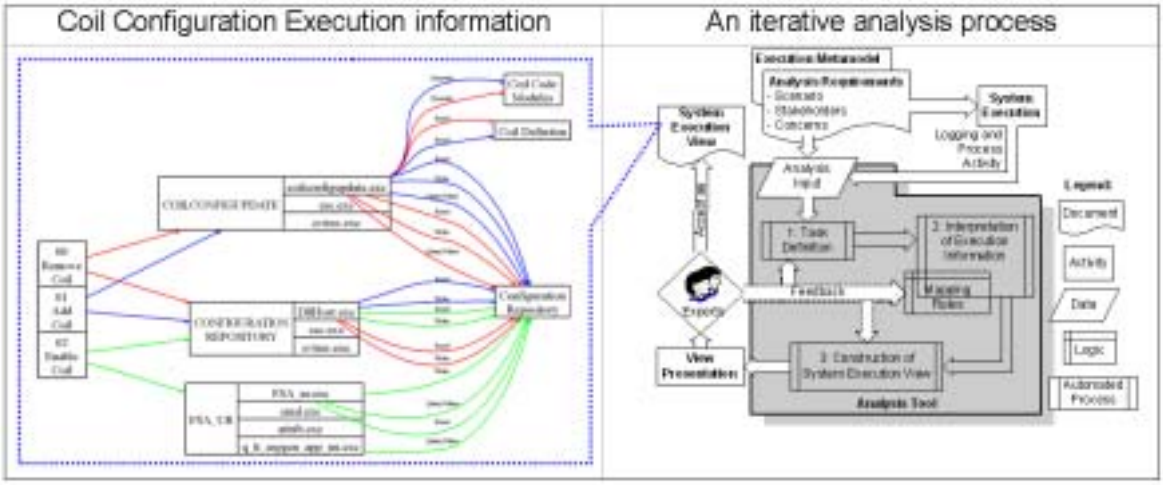
- Research:
  controller stability & robustness
- Other applications:
  environment & state recognizers

12 Top-down recovery of the MRI execution architecture

PHILIPS university of groningen

Overview

The Darwin project aims at improving the evolvability of complex software-intensive systems, in particular MRI scanners. One part of Darwin focuses on the recovery of the execution architecture from an actual running system. Software architects and designers developing large software-intensive systems usually follow informal top-down strategies to keep system knowledge in their minds as high-level mental models, and use them as the main source of information for their regular activities. However, due to the complexity of large software-intensive systems, mental models may not be always up-to-date.



Method

The method on show presents a top-down strategy to help software architects and designers in the creation and maintain of high-level mental models of the actual execution architecture of the MRI software. This strategy, as an iterative process synchronizes and analyzes two sources of execution information (system logging and process monitoring). The synchronization and analysis link high-level abstractions (scenarios, tasks, and components) with actual execution activities (data access, code execution, and platform utilization). The method is illustrated with a case study to identify coil-related dependencies in the execution of the MRI software. In the application, a set of requirements helps to manage complexity and focus the analysis in solving a specific problem. Generated views are validated based using experts' feedback and made available to help more software architects and designers in creating mental models about coil-related dependencies in the execution of the MRI software.

Benefits

This method benefits software architects and designer in maintain up-to-date and expand their current mental models about the system execution. With up-to-date and reliable mental models (i.e. about the system execution structure, its components and their dependencies), software architects and designers can be aware of the impact of changes, and react quick and efficient within the planning and execution of change and maintenance activities.

For more information

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Pierre America — ESI and Philips Research — pierre.america@philips.com

PHILIPS

university of groningen

Embedded Systems INSTITUTE

Darwin: The MRI Execution Architecture

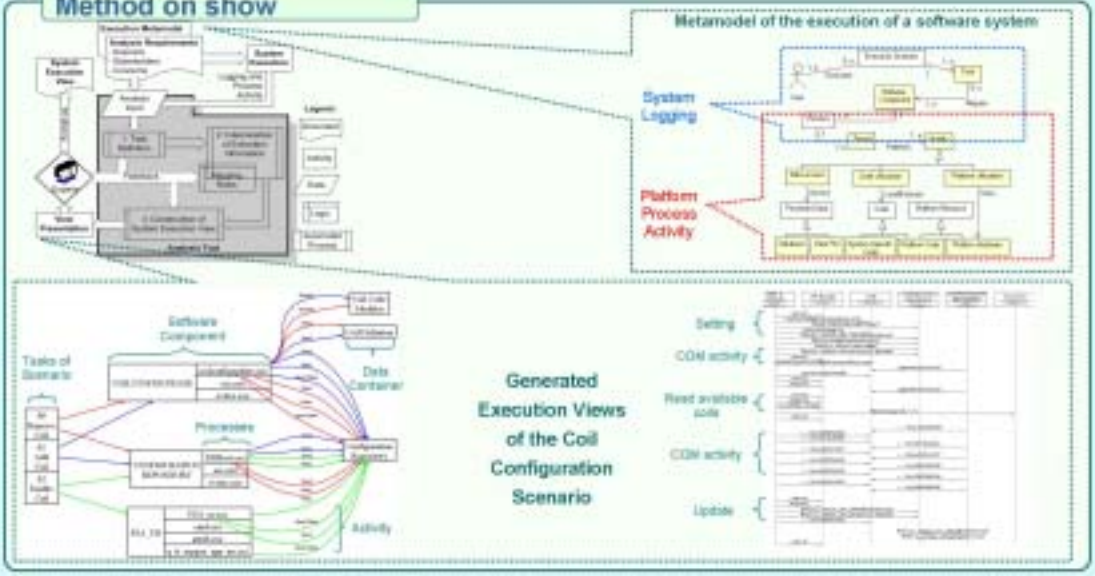
Trosky B. Callo
Pierre America

Research topic

- How to help software architects and designer in creating reliable mental models of the actual execution architecture of the large and complex MRI software.

- Identification of sources and techniques to gather high level system execution information.
- Efficient diagrammatic description of the actual runtime system structure and behavior.
- Manage information complexity at the high level and provide detail when needed.

Method on show



Projected benefits / value

For software architects and designers:

1. Identification of system components and their dependencies at the high level of abstraction.
2. Maintenance and expansion of current mental models about the execution of the system.
3. Understanding of the realization of the current implementation towards the creation of mental models.

For the MRI development organization:

1. Awareness on the impact of changes and fast reaction within the planning of change and maintenance.

Place in Darwin

Further research planned

- Evaluation of alternative sources and techniques to collect execution information.
- Improving diagrammatic representations for navigability and aggregation.
- Evaluation of current vs. recovered knowledge

13 Installed base visualization

Overview

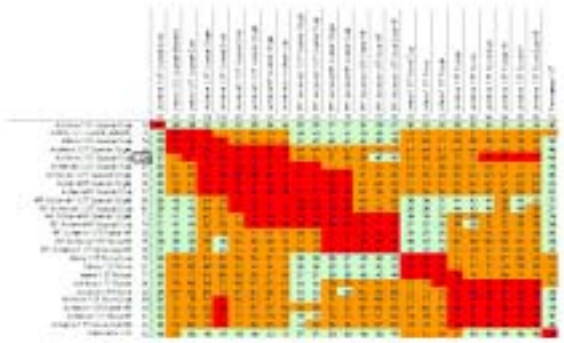
Knowing which configurations are installed around the world is needed to answer many different business-related questions. To give a few examples:

- When a part is no longer available, which configurations must be tested with the replacement to optimize the costs?
- Could the service costs be reduced by upgrading part of the installed base, i.e., by increasing the similarity between installed configurations?
- Given the test configurations and the potential pilot sites, which pilot site would yield the most information?

Currently, the data available in databases and spreadsheets about the installed base is not processed into useful information. As a consequence, decisions related to the installed base are taken based on experience and gut-feeling.

Method

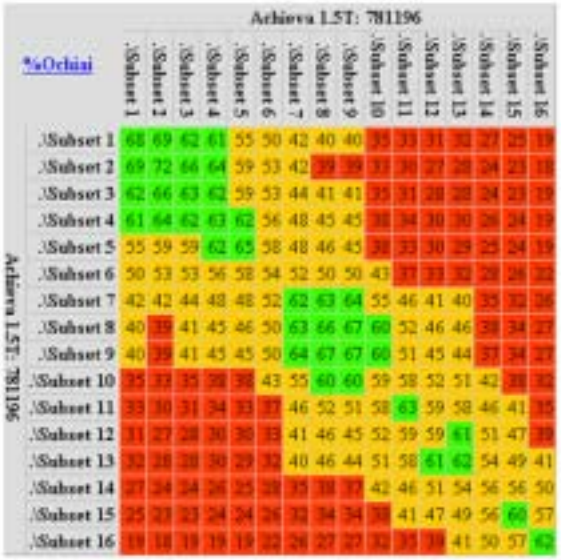
We visualize the installed base by exploiting the data available in databases and spreadsheets. This shows similarities and differences between different (sets of) configurations. Defining the similarity between configurations as a function of the number of the parts they share and the number of parts that each configuration contains, we can, for example, visualize how MRI systems have evolved over time.



127 orders in INTERA ACHIEVA 1.5T NOVA: 781172

58 orders in INTERA ACHIEVA 1.5T NOVA-DUAL: 781173

64 shared parts



nr	description	#Pairs	INTERA ACHIEVA 1.5T NOVA: 781172	INTERA ACHIEVA 1.5T NOVA-DUAL: 781173
989603011701	GRAD AMP C271-C	7366	127	58
989603011571	RF AMP 1.5T S23	7366	127	58
989603010661	D.S. PRE-ASSY PT6000 S	7366	127	58
989603010651	ADD GRAD AMPL C271 MASTER	7366	127	58
989603030762	PATIENT HEADSET >=R6.2	7366	127	58
989603036312	QRC EL-LOAD ACS-MT	7366	127	58
781036001	ALGEMEEN 1.5T	7239	127	57
781039002	MR ALGEMEEN	7239	127	57
989603011723	PFEI-C 1.5T	6930	126	55
989603011463	GRAD QRC COMB -1.5T-INF2	6188	119	52

Benefits

Visualizing the installed base by exploiting the data in databases and spreadsheets provides valuable insights. This can be improved by collecting additional data, and by developing specific visualizations geared towards answering particular questions. Although the installed base visualization is developed for Philips Healthcare MRI, the principles are generic, and valid for every modality within Philips Healthcare.

For more information

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PHILIPS

Embedded Systems INSTITUTE

Installed Base Visualization

Piërre van de Laar

Cost of Complexity

- What MRI configurations are operational?
  What differences exist? What parts are shared?

- Part no longer available (e.g. supplier bankrupt)
  On which configurations should a replacement be tested?
- What upgrade increases the similarity in the installed based, i.e., reduces the service costs?

Current Status @ PH-MRI

- Relevant data spread over multiple databases, spreadsheets, …
  - Incomplete and inconsistent
  - Geared towards service, sales, and logistics

- Decisions taken from experience & gut-feeling
  - Available data is NOT used

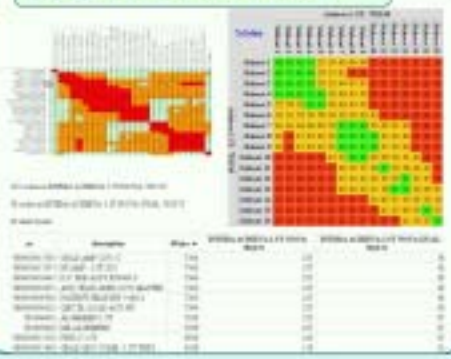
Similarity Measurement

- Configurations contain a large number of parts
- Similarity between configurations:

$$\frac{\#\,Parts\ Shared}{\sqrt{\#\,Parts\ in\ A}\sqrt{\#\,Parts\ in\ B}}$$

- Relevance of parts depends on question about installed base

Insight in Installed Base



Place in Darwin

Concept Proven

- Not limited to MRI,
  but generic for Philips Healthcare
- Exploits available data
  - Answers to questions related to installed base
  - Insight in what data to collect for future usage
- To be geared towards specific questions
  - Pilot site selection
    Site most different from test-configurations
  - Test configurations selection
    Lowest risk over all configurations

Innovation programmes and ESI

GENESYS

GENeric Embedded SYStem Platform
European Community's Seventh Framework Programme [FP7/2007-2013] n°213322

01/01/2008 - 30/06/2009

COOPERATION

The goal of GENESYS is to develop a blueprint for a European cross-domain architecture for embedded systems which is suitable for multiple application domains.

BENEFITS of a CROSS-DOMAIN ARCHITECTURE:

- Optimal support for a converging application world
  - new application scenarios (e.g., advanced in-vehicle electronics including control functions, consumer electronics, telematics, and communication technology)
  - ease the integration of subsystems
- More uniform knowledge profiles for embedded systems engineers
- Take advantage of the economics of scale in the semiconductor industry
- Avoid fragmentation through a cross-domain development approach
  - cross-domain platform services
  - cross-domain development tools

PROJECT PARTNERS

- Vienna University of Technology, Institute of Computer Engineering
- STMicroelectronics S.r.l.
- Commissariat à l'Energie Atomique
- Nokia Oyj
- Thales
- Embedded Systems Institute
- IMEC
- Technische Universität Darmstadt
- Fundacion European Software Institute
- VTT
- Infineon Technologies AG
- Centro Ricerche Fiat S.C.p.A
- TTTech Computertechnik AG
- Alma Mater Studiorum - University of Bologna
- Université Joseph Fourier Grenoble 1
- Fraunhofer-Gesellschaft zur Förderung der angewandten Forschung e.V.
- Technische Universität München
- Aytemiz Dizbioo Universitelisi
- Kentan S. Coop.
- Budapesti Muszaki es Gazdasagtudomanyi Egyetem
- Universidad Politecnica de Madrid
- NXP Semiconductors Netherlands B.V.
- Volvo Technology AB

GENESYS CONTEXT

Key challenges identified within ARTEMIS will drive the GENESYS project:

- **COMPOSABILITY**
  A concept that relates to the ease of building systems out of subsystems. A system, i.e., a composition of subsystems, is considered composable with respect to a certain property if this property, given that it has been established at the subsystem level, is not invalidated by the integration (p.8, ARTEMIS SRA report).
- **ROBUSTNESS**
  capability of a system to deliver an acceptable level of service despite the occurrence of transient and permanent hardware faults, design faults, imprecise specifications, and accidental operational faults (p.17, ARTEMIS SRA report).

- **POWER/ENERGY EFFICIENCY**
  - efficiency, for example in regard to low operating and standby power, and integral management of resources e.g., power, time (scheduling), communication bandwith, memory, and others (p.19, ARTEMIS SRA report).
  - significance of power and energy savings in embedded systems is constantly increasing (e.g., mobile devices, reduction of thermal stress, ecological solutions).

CHALLENGES OF THE TARGETED APPLICATION DOMAINS

CONSUMER APPLICATIONS

Contemporary embedded systems development in the nomadic environments and private spaces is driven by several pervasive trends, such as increasing processing capability, digital convergence and content or the integration with services in other environments such as shops or cars. The present-day architectural concepts and design methods are not well suited to support these developments.
Challenges include the seamless utilization of multiple network technologies to access remote or local services or the holistic resource management conserving the available battery power or maximizing the quality of the accessed media.
Competition pressure and productivity improvements require decreasing reaction times and product development times, but these are increasingly difficult to achieve. Furthermore, it is quite difficult for many IP vendors to offer pieces of designs that seamlessly fit with proprietary embedded architectures.

INDUSTRIAL APPLICATIONS

The GENESYS project will consolidate the different approaches currently used in the automotive, avionic and industrial control area and will bring about the following contributions, which are solutions to key challenges in all considered industrial domains:

- **Complexity Management**: The strict partitioning of a distributed service provision into communication components and computational components with a clearly defined interface in-between, will lead to a wide reuse of components and the reduction of the complexity at the system level.
- **Specification methodologies**: The cross-domain development methodology will consider the requirements on development and (parallel-) programming for the development in the industrial domains.
- **Certification**: The cross-domain architecture will take into account existing certification standards and recent advances in aerospace certification like for instance the ongoing work on new certification RTCS DO 178 standard (i.e., DO-178C).

SOLUTION

CONSOLIDATED CROSS-DOMAIN ARCHITECTURAL STYLE

- Rules and guidelines for the partitioning of a system into sub-systems and for the design of interfaces
- Alignment of different views, concepts, and design principles from different application domains
- Definition of architectural principles (e.g., ensuring error containment, partitioning of the system along precisely specified interfaces)
- Avoidance of property mismatches: components must comply with the architectural style to avoid a property mismatch at the component interfaces
- The architectural style constrains an architecture in such a way that the resulting system meets the ARTEMIS challenges

CROSS-DOMAIN DEVELOPMENT METHODOLOGY

- modeling, evaluation and validation of platform services and embedded systems based on the reference architecture template
- measurable quality characteristics

REFERENCE ARCHITECTURE TEMPLATE

- description of platform services
- generic component libraries
- platform service specifications e.g.,
- communication services, diagnostic services, security services, and resource management/reconfiguration services

www.genesys-platform.eu **office@genesys-platform.eu**

GENESYS

GENeric Embedded SYStem Platform
European Community's Seventh Framework Programme [FP7/2007-2013] n°213322
01/01/2008 - 30/06/2008

COOPERATION

This poster describes the structuring of embedded systems according to the GENESYS cross-domain architectural style. The GENESYS cross-domain architectural style encompasses fundamental architectural principles for robust embedded systems. Robustness concerns the handling of transient and permanent failures in the hardware, design faults in the software and intrusions. The cross-domain architectural style has been defined through a convergence of architecture views and concepts across the application domains.
Each principle of the architectural style is an accepted statement about some fundamental insight in a domain of discourse. Principles form the basis for the formulation of operational rules. In GENESYS these principles are operationalized in the reference architecture template of the architectural service specification.

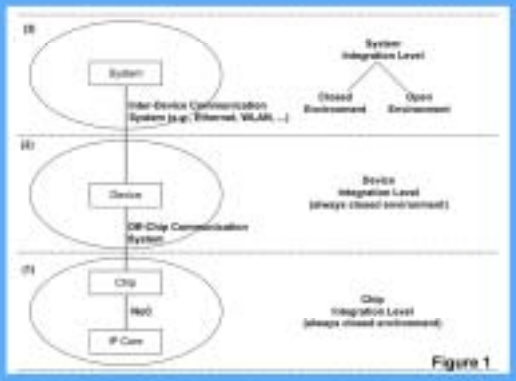


Figure 1

The GENESYS architecture introduces three different integration levels: the *chip-level*, the *device-level*, and the *system-level* (see Figure 1). At the system level *open* and *closed systems* are distinguished. At each level, the architecture provides *core services* and optional *services*.
The reason for the introduction of these integration levels is that the service characteristics of the three levels are substantially different, e.g., the bandwidth in a network-on-chip (NoC) is orders of magnitude cheaper than the bandwidth at the system level (e.g., WLAN). A major reason for distinguishing open and closed systems is that temporal guarantees can only be given in a closed system.

Figure 2 depicts the component interface structure. It is distinguished between the local interfaces and the linking interfaces (LIFs) of a component. The LIFs are the interfaces for the integration of components at a given integration level (i.e., inter-device LIF, inter-chip LIF and inter-IP core LIF). The LIF of a component abstracts over the internal structure and local interfaces of the component. The LIFs need to be technology independent in the sense that the LIF does not incorporate implementation details of a component. A technology independent LIF ensures that different implementations of computational components can be integrated (e.g., general purpose CPU, FPGA, ASIC).
Local interfaces are interfaces to the component environment (e.g., using sensors and actuators) or to other subsystems (i.e., in case of a gateway). The local interfaces (e.g., technology-specific interface to transducer) of a component are not constrained by the LIF specification. However, the LIF specification includes those properties of the local environment that are of relevance for the integration.

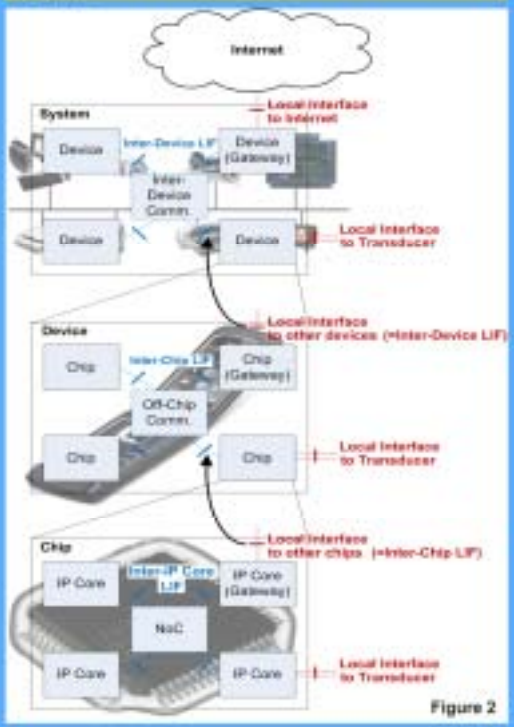


Figure 2

PROJECT PARTNERS

- Vienna University of Technology, Institute of Computer Engineering
- ETMicroelectronics S.r.l.
- Commissariat à l'Energie Atomique
- Ingeniia
- Thales
- Embedded Systems Institute
- IMEC
- Technische Universität Darmstadt
- Fundacion European Software Institute
- VTT
- Infineon Technologies AG
- Centro Ricerche Fiat S.C.p.A.
- TTTech Computertechnik AG
- Alma Mater Studiorum - University of Bologna
- Universite Joseph Fourier Grenoble 1
- Fraunhofer-Gesellschaft zur Förderung der angewandten Forschung e.V.
- Technische Universität München
- Vrije Universiteit Brussel
- Evidian S. Corp.
- Budapest Muszaki es Gazdasagtudomanyi Egyetem
- Universidad Politecnica de Madrid
- NXP Semiconductors Netherlands B.V.

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Competence Development Program for System Architects

Embedded Systems INSTITUTE

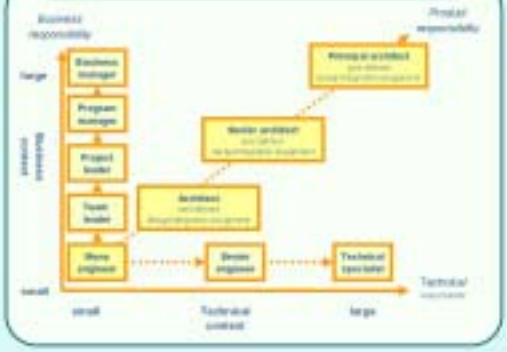
System-level professionals required

High-tech system industry trends:

- Function: Extension of functional capabilities
- Data: Extend information contents (memory)
- Cost: Reduction of cost-per-function
- Speed: Faster processing performance
- Power: More efficient power utilization
- Size: Smaller and more light-weight products
- Technology: Increase of new and changing technologies
- Integration: Integration of functions/components/ technology

Innovation effort increases due to growing complexity

System architect career path



Vision, mission & approach

Vision: System architecture is a key asset for embedded systems industry

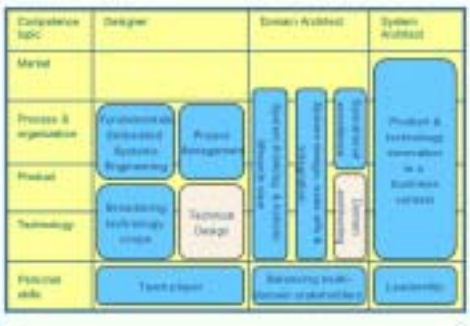
Mission: To provide a world-class Competence Development Programme for embedded system architects

Approach:

- 3 competence levels
- Content based on latest insights
- Top level teachers & coaches
- Combination of theory, practical assignments & networking
- Based on partnership with industry & knowledge providers

Broadening the scope

Competence profiles



Theory, practical assignments, network activities & coaching

	program stage I	program stage II	program stage III
Theory	Courses	Courses	Courses
Learning on the job	Practical assignment	Practical assignment	Practical assignment
Professional Network	Experience sharing	Multi-company working group	Visiting committees
Personal skills	Coaching	Personal coaching	Personal coaching

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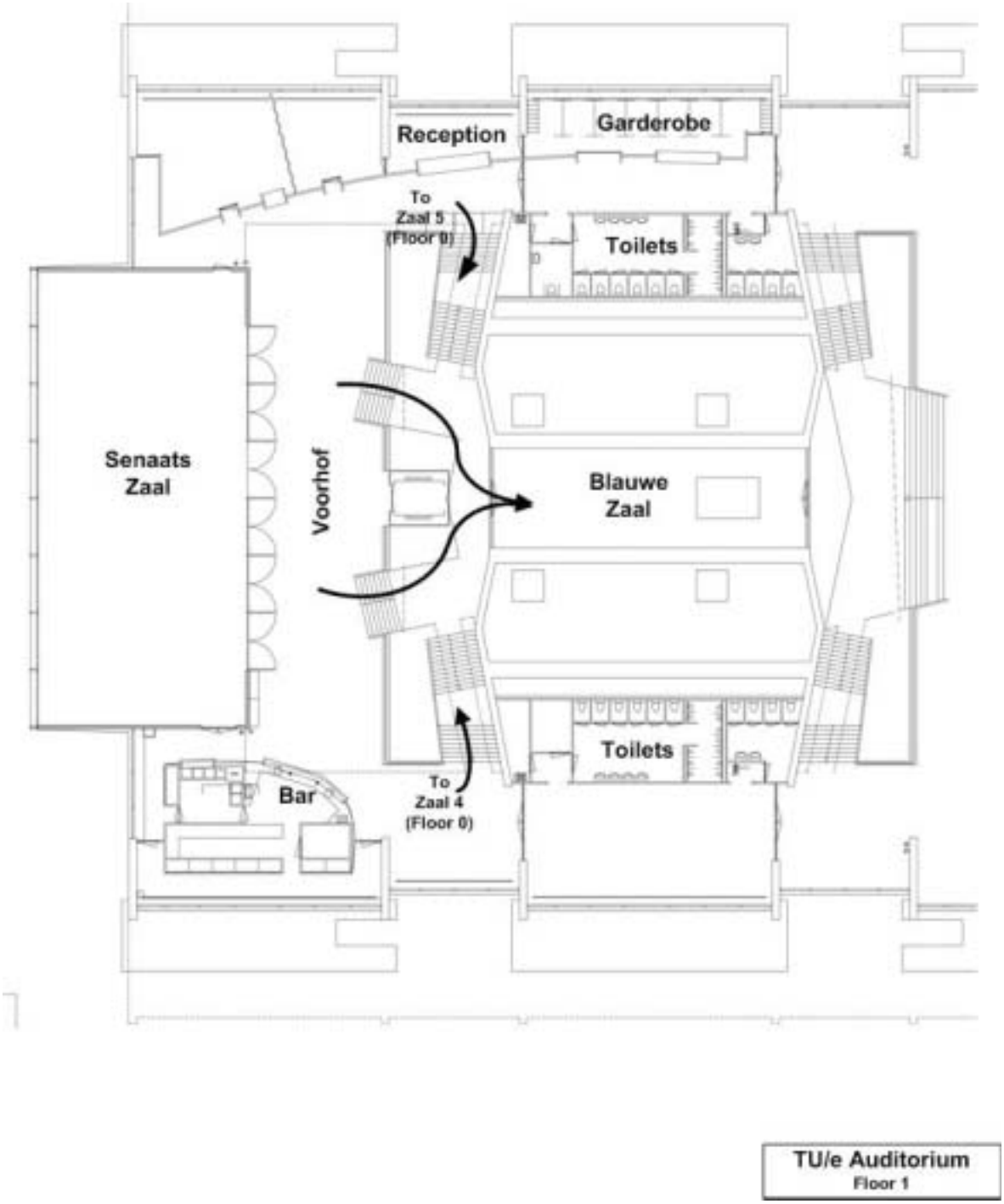
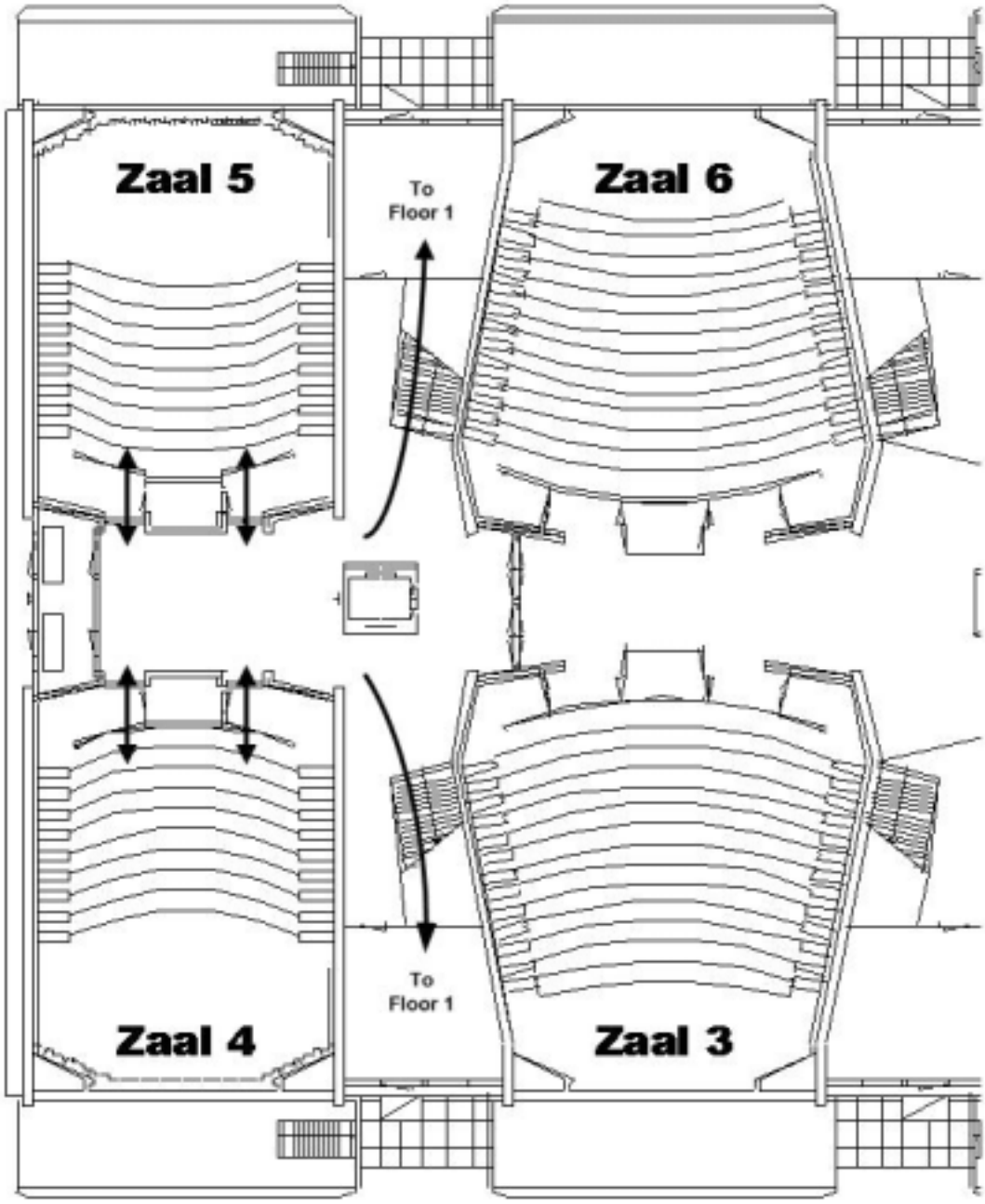
Auditorium plan

Main floor

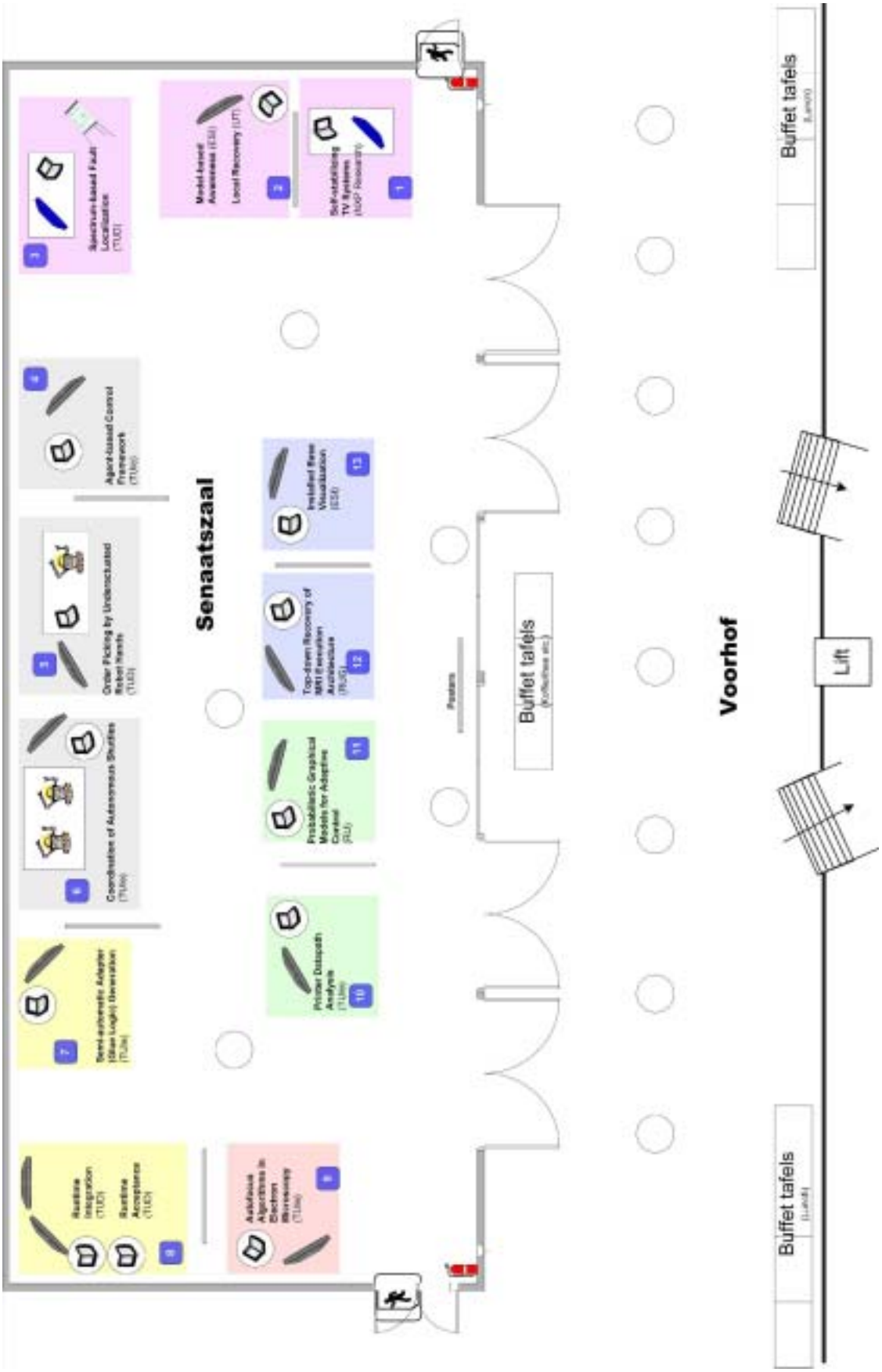


Presentations rooms



TU/e Auditorium
Floor 0

Info market room (Senaatszaal)



Programme

09:00	**Registration**, coffee & tea *Senaatszaal*			
09:30	**Welcome and opening — Ed Brinksma** *Blauwe zaal*			
09:45	**Keynote presentation — Lothar Thiele** *Blauwe zaal* Predictability and Efficiency in Wireless Sensor Networks			
10:30	**Break** (30 min), Information market *Senaatszaal*			
	Track 1 *Coll.zaal 4* **Trader**	**Track 2** *Coll.zaal 5* **Falcon**	**Track 3** *Blauwe zaal* **Quasimodo/Poseidon**	**Info market** *Senaatszaal*
11:00	*Jozef Hooman:* User Perceived Reliability of high-volume products	*Jurjen Caarls:* System Level Control of Warehouses	*Kim Larsen:* Quasimodo	Demos
11:30	*Arjan van Gemund:* Fault Diagnosis of Embedded Systems	*Roelof Hamberg:* Dependable robotic Subsystem Design for Distribution Centers	*Michael Borth:* Building Dynamic Information-centric Systems-of-Systems	
12:00	**Lunch** (1 hour), **Information Market** *Senaatszaal*			
13:00	**Track 4** *Coll.zaal 4* **Darwin**	**Track 5** *Coll.zaal 5* **Dependability (3TU)**	**Track 6** *Blauwe zaal* **Progress**	**Info market** *Senaatszaal*
13:00	*Rolf Theunissen:* Supervisory control synthesis for a patient support system	*Arie van Deursen:* Introduction to the track	*Bart Theelen:* Performance Model Generation for MPSoCs with Resource Management	Demos
13:10		*Jaco van de Pol:* Dependable Railway Infrastructure		
13:20	*Ana Ivanovic:* The value of investments in evolvability			
13:30		*Sandro Etalle:* Securing Information in Systems of Systems	*Andy Pimentel:* Daedalus: Towards Composable Multimedia MP-SoC Design	
13:40	*Pierre America:* Top-down Generation of Execution Architecture Views…			
14:00	**Break** (15 min) *Senaatszaal*			
	Track 7 *Coll.zaal 4* **Trader**	**Track 8** *Coll.zaal 5* **Valorization**	**Track 9** *Blauwe zaal* **Progress**	**Info market** *Senaatszaal*
14:15	*Hasan Sozer:* Decomposing Software Architecture to Introduce Local Recovery	*Christian Bakker:* Diagnosis of Wafer Stage Failures	*Stefan Dulman:* Featherlight collaborative ambient systems	Demos
14:45	*Jeroen Keijzers:* Measurement and Analysis of User Perception of Picture Quality Failures	*Joris van den Aker:* Experiences with Technology Transfer	*Marcel A. Groothuis:* ViewCorrect: Embedded Control Software design using a model-driven method	
15:15	**Break** (30 min), Information market *Senaatszaal*			
15:45	**Keynote presentation — Anton Schaaf** *Blauwe zaal* Innovation acceleration, the way with ESI			
16:15	**Future plans** and closure — **Ed Brinksma** *Blauwe zaal*			
16:45	**Drinks** *Senaatszaal*			

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